Logic Analyzer Connectorless Probing Reduces Loading and Footprint Impact on DDR Memory Validation

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DDR memory has emerged as the leading technology for in-system DRAM. Verification of DDR systems has also emerged as one of the most challenging and time consuming tasks of modern digital system design. Logic analyzers are key in assisting engineers with the verification of these systems. However, with the cost and spatial constraints being imposed on designers, logic analyzer probing is becoming a concern.

In an ideal world, DDR testability would be part of the final design. This would allow test-bench verification of the system as cost engineering and outsourcing occurs over the life of the product. However, this has not been practical until today due to electrical loading and space requirements of logic analyzer probe points. New connectorless logic analyzer probing is allowing DDR testability to be incorporated into the initial and final stages of a product with little impact on cost, board space, or signal integrity.

Connectorless Probing

Recently, logic analyzer vendors have introduced a new class of probes called "Connectorless". These new probes use compression interconnect technology that removes the need for a connector on the target. Instead of a connector, small landing pads are placed on the target PCB. The electrical interconnect of the probe is then compressed onto the pads making electrical contact. The reduced footprint from removing the connector means that minimal space is needed to incorporate logic analyzer testability. In addition, removing the connector reduces the overall load of the probe. The low electrical loading of the probe (<0.7 pF) means that when the probe is connected, the signals are not electrically disturbed. Also, since a connector does not physically reside on the target PCB, when the probe is not connected, only the landing pads remain. These pads are electrically insignificant (~80fF). This means that leaving the logic analyzer testpoints in the final production design is now practical.

DDR Systems

One of the most popular implementations of DDR memory is using a socketed DIMM. Designers place multiple 184-pin DIMMs side-by-side and share the memory bus to increase storage capacity. This implementation is used widely in computer systems due to its scalability. While this implementation seems straight forward, there are many considerations and constraints that must be addressed by the system designers.

The first consideration is spatial. Designers do not have an infinite amount of PCB space available. Thus, the memory system must be implemented in as little space as possible.

A second important constraint is cost. The main impact of cost is in the reduction of layers on the target PCB. Many DDR systems are being implemented on 4-layer PCB's that have only two signal layers. While DDR sockets are pinned out for this style of routing, it is challenging to accommodate miscellaneous circuitry that is also needed by the DDR system.

Another problem faced by designers is signal integrity. The sheer number of signals and high data rates, make a DDR system a very difficult implementation. When adding the additional constraint that there are only two routing layers and that the system must be as small as possible, designs are continually running out of margin.

A final but important consideration is testability. With all of the above constraints on designers, there is usually little space or margin in the system to incorporate testability. However, testability is key to the validation and time-to-market for the product. To exacerbate this situation, designs are often changed or cost engineered during the life of the product. When a product is changed in production, there needs to be a quick and reliable method to validate that the changes have not altered the original functionality of the design. Until now, leaving testability in the production design was not an option due to electrical loading and the space/routing required. However, with connectorless logic analyzer probing all that has changed.

Using Connectorless Probing for DDR Validation

Connectorless logic analyzer probes lend themselves very nicely to DDR system debug. The main reasons are the reduced footprint size, low loading when connected, negligible loading when not connected, and the flow-through routing capability. To illustrate the power and versatility of this style of probing, consider the following memory system when outfitted with connectorless probes like the SoftTouch probes from Agilent Technologies.

The following figure shows an example layout of a DDR system using four Socketed, 184-pin DIMMs. This system is double terminated with the connectorless probes placed between the terminations (midbus probing). This figure is showing the topside routing for all 2x signals (data and stbs). The 1x signals (address and control) are routed in a similar fashion on the bottomside of the board. Each SoftTouch footprint contains 34 channels of testability. It takes three footprints to test the 2x data in the DDR system. The bottomside of the PCB contains two SoftTouch footprints to test all of the 1x DDR signals. To understand the power of the connectorless probes, the incremental impact on the system should be explored.

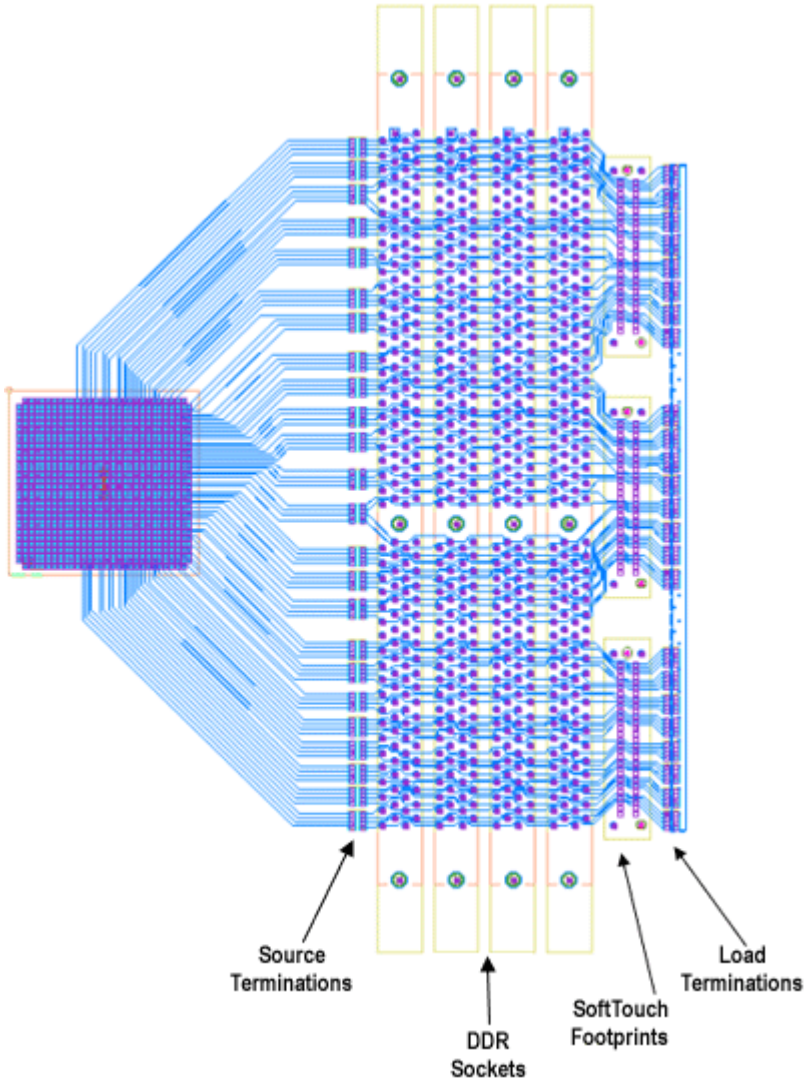

Figure 1: Example layout for SoftTouch probing of a DDR system (Showing only Topside 2x Data)

Spatial Impact

Adding the connectorless probe footprints increases the space needed by memory system by an additional 0.390-inch in the X-axis. Said another way, the load termination resistors have to be placed an additional 0.390-inch from the last DIMM socket. If the relative size of the memory system is measured from the leftmost trace coming out of the driver IC to the rightmost edge of the load termination resistors, the corresponding increase due to the connectorless probe footprints is less than 10%.

Another exciting benefit of the connectorless probes is the flow through routing capability. The footprint and pinout of the logic analyzer probe is such that signals can traverse the testpoints without having to change layers. This means that in a DDR system, no additional layers are needed to incorporate logic analyzer testability. This is crucial to a system implemented on a four-layer board.

Electrical Impact

In the above example, the additional testability reduces the signal integrity of the system. When weighing the importance of testability versus the margin reduction, the question becomes "how much is the margin reduced?"

A typical four-layer DDR system uses 0.005-inch trace widths routed on the outer layers of the PCB. These layers are designed to be 50 Ohms. For this type of microstrip trace, this corresponds to ~3pF/inch of capacitance. To examine how much additional loading is present due to the logic analyzer probes, consider the cases when the probe is connected and when it is not connected.

CASE 1: When the probe is connected

Additional trace due to testability	= 0.390"
Parasitic Capacitance of trace	= (0.390") * (3pF/inch) = 1.17pF
Additional Probe Capacitance	= 0.7pF (NOTE: This includes the pads)
Total excess capacitance due to testability	**= 1.17pF + 0.7pF = 1.87pF**

CASE 2: When the probe is NOT connected

Additional trace due to testability	= 0.390"
Parasitic capacitance of trace	= (0.390") * (3pF/inch) = 1.17pF
Additional probe pad capacitance	= 80 fF
Total excess capacitance due to testability	**= 1.17pF + 0.08pF = 1.25pF**

To understand if this capacitance is of concern, a first order analysis of the system must be done.

Capacitance of DDR system as seen by driver

Total trace length of original system	= 2.767" (NOTE: Using longest 2x trace)
Parasitic capacitance of trace	= (2.767") * (3pF/inch) = 8.3pF
Lumped capacitance of DIMM	= 5pF (NOTE: DDR333, DQ, DQS, DM)
Number of DIMMs on bus	= 4
Capacitance due to DIMMs	= (4) * (5pF) = 20pF
Total capacitance of DDR System	**= 8.3pF + 20pF = 28.3pF**

This first order analysis shows that when the probe is connected, it only adds an incremental 6% to the capacitance that the driver sees. Even more importantly is that when the probe is not connected, the testpoints and traces left on the PCB only add an incremental 4%. This means that leaving the connectorless footprints on the final production design will not significantly degrade the signal integrity of the system. The benefit of having testability incorporated into a shipping product is extremely valuable and well worth the 4% margin reduction.

Cost Impact

Since there is no connector needed for the testpoints, there is no incremental cost to the final bill of materials for the product. This means that having this built-in DDR testability is for all intensive purposes free.

Conclusion

When designing fast-cycle time products, there is always the challenge of trading off testability vs. schedule and margin. Having solid testability requires forethought and planning in addition to PCB space and system margin. However, solid testability will ultimately reduce time-to-market. DDR systems are a prime example of these engineering tradeoffs. It has always been a struggle to justify incorporating permanent logic analysis testpoints into a design due to the PCB space, routing layers,

and connector cost. With the advent of connectorless logic analyzer probes, the justification has become much easier. Now a DDR system can be fully tested in the final design with little impact to the size, signal integrity, or cost of the system.

About the Author

Brock J. LaMeres received his BSEE from Montana State University in 1998 and his MSEE from the University of Colorado in 2001. He is currently working on his Ph.D. at the University of Colorado where his research focus is High-Speed IO for next generation ICs. LaMeres is a hardware design engineer for Agilent Technologies in Colorado Springs where he designs logic analyzer probes and high-speed transport systems.

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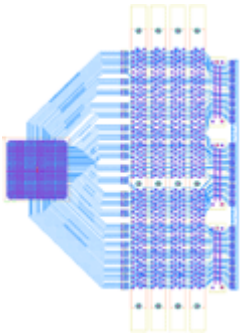

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