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Physical Connections are Key in FPGA Debug

Without a sound electrical connection, the best, most sophisticated debug tools are useless. Designers can choose from among three methods to achieve robust connections.

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Digital system designers are turning to FPGAs as their main building blocks due to their flexibility and scalability. They've become the key enabler for configurable computing architectures. But debugging an FPGA is still one of the most time-consuming tasks that a designer faces during the development cycle. Many powerful logic analysis tools exist to aid validation teams in debugging FPGA problems quickly. That said, the most powerful logic analyzer is useless without a sound electrical connection to the device under test (Figure 1). Intermittent connections can cause designers to chase errors that are solely due to the electrical connection between the FPGA design and the logic analyzer.

There are a number of ways to make a successful logic analyzer connection to an FPGA. The three most recent connection/debug schemes are external connector-less, internal dynamic and forgotten signal probing. Ensuring successful logic analyzer connectivity requires careful attention to the physical implementation.

External Connector-less Probing

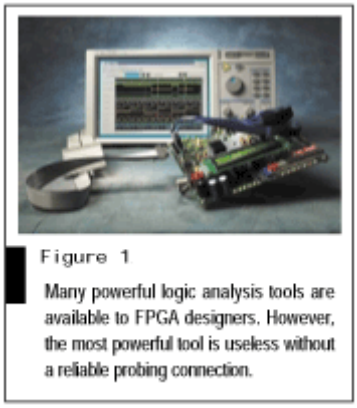

Figure 1
Many powerful logic analysis tools are available to FPGA designers. However, the most powerful tool is useless without a reliable probing connection.

The first type of probing connection for FPGA debug is using connector-less technology. Connector-less probing refers to a technology that removes the connector from the target PCB. Instead, landing pads are placed on the target to which FPGA signals are routed. The probe tip consists of a compression interconnect. Through the use of a retaining device, the probe tip interconnect is compressed and aligned onto the landing pads on the PCB completing the electrical connection.

This new technology has many advantages. The first is the electrical advantage of removing the connector from the PCB. By removing this physical structure from the probing connection, the capacitive loading is reduced over traditional connector probes. Capacitive loading has been reduced from 3pF on the Mictor probe to 0.7pF on the connector-less probes. The second advantage is the logistics of not having to load a fine-pitched connector on the target PCB. The cost of the connector and not having to procure the parts make this a hidden treasure of connector-less probing. Finally, the landing patterns of the connector-less probes are such that signals can route through the pattern. This has the advantage in that high-speed signals can be probed in their native routing environment, thus making a more accurate and less perturbing measurement (Figure 2). This is an improvement over connector probes that traditionally block flow-through routing, requiring placement to the side of the routing channels and stub traces to be used.

Internal Dynamic Probing

Another analysis tool available to FPGA designers is the dynamic probe, co-developed by Agilent Technologies and Xilinx. This new technology allows designers to integrate a probing core into their FPGA designs that will dynamically route internal nodes of the design to a debug port that is observed

using a traditional logic analyzer. Up to 64 internal nodes can be selected for observation on an individual debug channel.

The dynamic selection of the internal nodes is controlled using a standard JTAG programming cable and does not require a recompile of the FPGA design. The software that runs the JTAG interface resides on the logic analyzer mainframe that is concurrently probing the debug port of the FPGA. This allows one logic analysis application to choose, acquire and display the internal nodes of the FPGA.

The physical connection for this type of debug requires two ports to be added to the target. The first is the standard JTAG connection. This header is typically included in designs for prototyping so it does not add incremental effort. The second port that is added is the debug port used to bring the internal nodes out to the logic analyzer. Any style of logic analyzer probe can be used to observe this port. Connector-less probing technology lends itself well to this type of non-intrusive debug.

There are very few electrical considerations for the debug port in order to provide an easy to use tool for the designer. The signals of the dynamic probe require no external components for terminations. In addition, the logic analyzer has the ability to calibrate out channel-to-channel skew so trace matching is not needed. The only consideration is to keep the debug port as close to the FPGA as practically possible and route using controlled impedance transmission lines when running the debug port at high data rates—greater than 50 Mbits/s. Both of these factors are usually inherent in designs using complex FPGAs.

The number of channels on the debug port is at the discretion of the FPGA designer. As mentioned previously, up to 64 internal nodes can be selected for observation on an individual debug channel. One powerful feature of the FPGA dynamic probe is that it allows a 2x multiplexing of the internal nodes onto the port. This means that the number of internal nodes that can be observed simultaneously is 2x of the number of physical channels on the debug port. Since the multiplexers are configured and controlled by the JTAG interface software that resides on the same logic analyzer machine as the logic analyzer acquisition, this multiplexing is seamless within the analyzer application and display. Now probing points can be changed in seconds instead of hours by eliminating the need to recompile the design.

Connection to Forgotten Signals

One of the most common issues that designers encounter when using logic analysis is that they forget to bring out all of the signals of interest to an observation point. Even when designers plan ahead and put down the appropriate features on the PCB—such as connector-less footprints—inevitably there are always a couple more signals that could make the debug easier. To aid designers in this situation, logic analyzer vendors have created a probing interconnect known as a flying lead. The flying lead is an individual probing channel at the end of a cable. This type of probing is very similar to oscilloscope probing.

Figure 3
FPGA signals in a BGA package that were not brought out to a logic analyzer test point can still be observed using a damped-wire accessory and a flying

The density of modern FPGAs has pushed them almost exclusively into grid-array style packaging. This type of packaging is advantageous for signal density but prevents easy access to signals that are not explicitly brought out to test points. The only observation point is at the PCB breakout via pattern beneath the FPGA package. Advances in the flying lead probing technology have allowed FPGA designers to connect to signals in a grid-array package by soldering to the breakout vias.

The process for making this type of connection is to first remove the soldermask from the breakout via of interest. This is easily accomplished using an Exacto-knife or something similar. Once the bare copper is exposed, a solder connection can be made from the probe to the breakout via. Modern flying lead probes come with accessories specifically designed for the purpose of soldering to small features such as a via. The accessory, known as a damped-wire, is soldered to the via and then connected to the flying lead probe completing the electrical connection.

The ability to probe forgotten signals that have not been brought out to a test point eliminates the need for elaborate work-arounds that FPGA designers typically turn to (Figure 3). This reduces

validation time and lets designers debug the original design instead of a modified prototyping version.

Another powerful use of this type of probing is in conjunction with the internal logic analyzer described above. As long as the JTAG signals are accessible, all of the features of the ILA are available using this type of probing.

More Efficient Validation

FPGAs are becoming the most widely used building blocks in digital systems. As with any design cycle, FPGA validation is a crucial and potentially time-consuming task that must be addressed. Engineers need robust tools to quickly and accurately debug their FPGA designs without worrying that they are chasing an error that could be due to an intermittent probing connection to the target. To assist FPGA designers, logic analyzer vendors have created a suite of interconnect/debug solutions that provide the robust physical connection between the analyzer and the target. Signals can now be observed external to the FPGA with minimal loading and routing disturbance using connector-less probing technology.

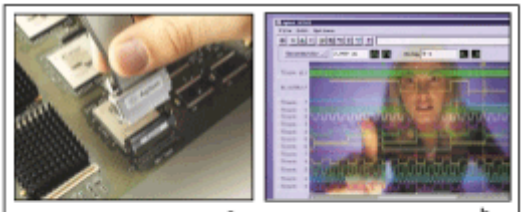

Figure 4

The internal logic analyzer from Agilent Technologies, Inc. allows internal nodes in an FPGA to be dynamically routed to a debug port without recompiling the design. Connector-less probes lend themselves well to this type of non-intrusive probing.

Internal nodes within the FPGA can be dynamically routed to a logic analyzer without recompiling the design using the FPGA Dynamic Probe from Agilent Technologies (Figure 4). And finally, forgotten signals can now be accessed using the new flying lead interconnect technology by directly soldering to the breakout vias of the grid-array FPGA packaging. These new ways to connect and debug an FPGA design mean that engineers no longer need to worry about making a successful probing connection or that the probe will distort the results of the measurement.

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