PHASE ALIGNMENT OF ASYNCHRONOUS EXTERNAL CLOCK CONTROLLABLE DEVICES TO PERIODIC MASTER CONTROL SIGNAL USING THE PERIODIC EVENT SYNCHRONIZATION UNIT

by

Charles Nicholas Ostrander

A thesis submitted in partial fulfillment
of the requirements for the degree

of

Master of Science

in

Electrical Engineering

MONTANA STATE UNIVERSITY
Bozeman, Montana

May 2009

APPROVAL

of a thesis submitted by

Charles Nicholas Ostrander

This thesis has been read by each member of the thesis committee and has been found to be satisfactory regarding content, English usage, format, citation, bibliographic style, and consistency, and is ready for submission to the Division of Graduate Education.

Dr. Brock J. LaMeres

Approved for the Department Electrical Engineering

Dr. Robert C. Maher

Approved for the Division of Graduate Education

Dr. Carl A. Fox

STATEMENT OF PERMISSION TO USE

In presenting this thesis in partial fulfillment of the requirements for a master's degree at Montana State University, I agree that the Library shall make it available to borrowers under rules of the Library.

If I have indicated my intention to copyright this thesis by including a copyright notice page, copying is allowable only for scholarly purposes, consistent with "fair use" as prescribed in the U.S. Copyright Law. Requests for permission for extended quotation from or reproduction of this thesis in whole or in parts may be granted only by the copyright holder.

Charles Nicholas Ostrander

May 2009

TABLE OF CONTENTS

TABLE OF CONTENTS - CONTINUED

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

LIST OF FIGURES - CONTINUED

Figure Page

LIST OF FIGURES - CONTINUED

Figure Page

LIST OF ABBREVIATIONS AND ACRONYMS

(ADC)	Analog to Digital Converter
(BW)	Bandwidth
(DFF)	D-Flip Flop
(DIP)	Dual Inline Package
(DSP)	Digital Signal Processing
(ECDL)	External Cavity Diode Laser
(ECL)	Emitter Coupled Logic
(EOPM)	Electro Optical Phase Modulator
(f)	Frequency
(FPGA)	Field Programmable Gate Array
(FM)	Frequency Modulation
(FT)	Fourier Transform
(GBPS)	Gigabits Per Second
(IC)	Integrated Circuit
(IFT)	Inverse Fourier Transform
(LCM)	Least Common Multiple
(MUX)	Multiplexer
(PCB)	Printed Circuit Board
(PECL)	Positive Emitter Coupled Logic
(PESU)	Periodic Event Synchronization Unit
(PFD)	Phase Frequency Detector
(PL)	Data Pattern Length
(PLL)	Phase Locked Loop
(PPG)	Pulse Pattern Generator
(PW)	Pulse Width
(Rev)	Revision
(RF)	Radio Frequency
(RMM)	Retriggerable Monostable Multivibrator
(RMS)	Root Mean Square
(SSB)	Single Side Band
SSH	Spatial-Spectral Holography
(SSOI)	Signal Set of Interest
(V_{pp})	Volts Measures Peak to Peak
($V_{OH(L)}$)	High (Low) Output Voltage

ABSTRACT

The Periodic Event Synchronization Unit aligns devices without the ability to be triggered by an external source. The primary function of the unit is to align the pattern trigger pulses of two pulse pattern generators which supply four inputs of a multiplexer. The pulse pattern generators lack the ability to start their code according to an external signal. When operating, the designed unit maintains a specific pattern alignment of two binary data streams of 5 gigabits per second as a multiplexer combines them into a data stream of four times the bit rate. In addition to alignment, the unit can introduce offsets of up to 50 nanoseconds to the pattern alignment which corresponds to 250 bits. The unit is designed to allow the alignment of other devices as well, requiring as input the two event signals of the same frequency which need to be aligned. In order to align the devices providing the event pulses, one of the devices must either accept an external clocking source or have the ability to frequency modulate the internal clock. In practice, the test system was able to achieve and maintain the desired signal characteristics from the output of the multiplexer. The unit's robust design is shown by providing alignment of patterns for the full operating range of the pulse pattern generators and allowing a generator pattern to be aligned to a generic event pulse. Use of multiple units allows alignment of additional devices. The development of the Periodic Event Synchronization Unit provided an inexpensive solution to creating very high bit rate signals using pre-existing equipment, as no commercial products were found to accomplish the same function.

INTRODUCTION

Project Overview

The impetus for the development of an event synchronization device was provided by a research effort to generate sets of digital microwave signals with 20GHz of bandwidth (BW) anywhere in the microwave spectrum up to 100GHz. Figure 1 provides an outline of the process explored for analog to digital conversion (ADC) of the microwave signals. The signal set of interest (SSOI) and a reference signal are modulated onto an external cavity diode laser (ECDL) by means of Electro-Optic Phase/Amplitude Modulators (EOPM). The signal and reference are then passed through a spatial-spectral holographic (SSH) material either collinearly or at an angle to create a grating that is either absorptive or diffractive in nature. The spectrum of the signal is obtained by digitizing a chirped optical source passed through the SSH material. The properties of the material allow the chirped signal to be captured at a far slower rate than a rate required to capture the original SSOI. Specific processing techniques are employed to recover the spectral absorption profile from the transformed chirp signal. This profile can then be manipulated with the Fourier transform (FT) of the reference signal to provide the signal of interest's Fourier transform, which can be inversed to produce a digitization of the original microwave signal. Above is a very basic introduction to the SSH-ADC project. A more complete description may be found within the Montana State University Spectrum Lab article Demonstrations of analog-to-digital conversion using a frequency domain stretched processor[1].

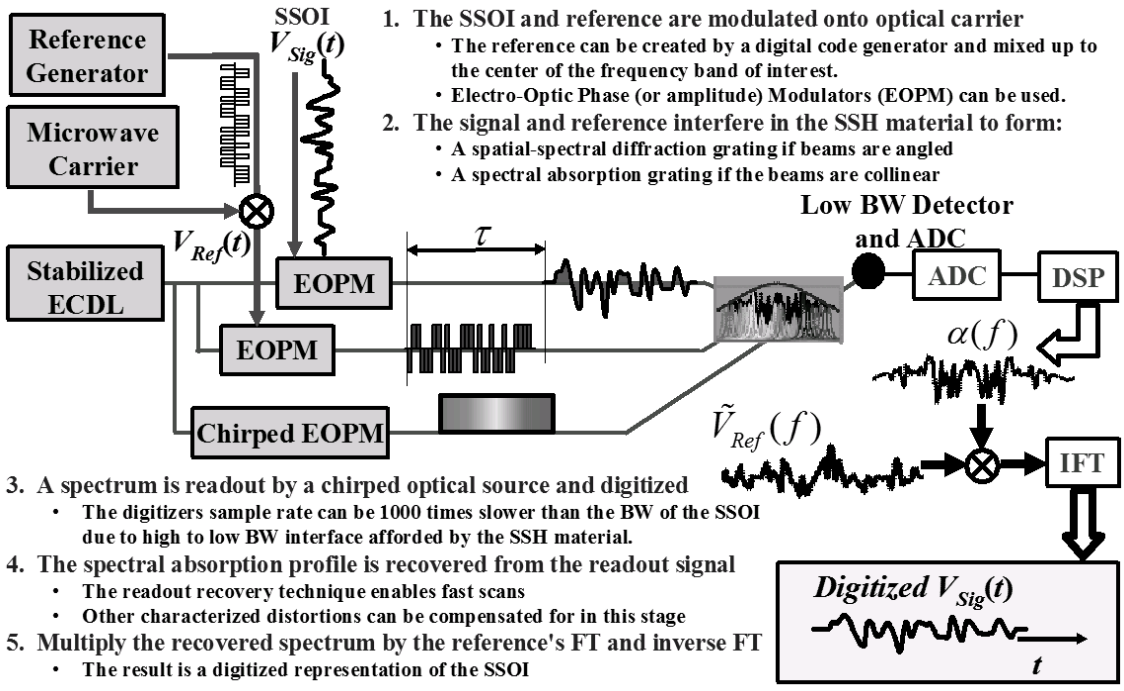


Figure 1: Proposed Means of Direct Digital Conversion of Microwave Signals

In this project, I developed an electronic synchronization unit for the alignment of the devices supplying the reference code pattern. This portion of the project required a unique means of electronic synchronization to accomplish the reference code generation. In order to improve the resolution for the digital conversion, the reference signal requires consistency in its temporal position. Timing jitter on the starting positions of the reference signal or bit to bit variations within the signal directly correspond to loss in signal to noise ratio of the digitizer's vertical resolution. To achieve the 20GHz bandwidth of the analog to digital converter (ADC), the process requires double-sideband readout of 10GHz gratings. A bit rate of 40GBPS for the reference signal is necessary to achieve this grating resolution. Commercial equipment, such as a bit error rate test unit operating at 40GBPS, is available[2] but the cost makes the units unsuitable for this

application. An alternative to buying a dedicated 40GBPS device is to use less expensive, lower bit rate devices and a multiplexer (MUX) to combine the patterns into a single stream at the required bit rate. An ***Inphi*** 40GBPS MUX chip with evaluation board[3] currently is priced less than $20k, which is at least one-tenth the cost of a dedicated 40GBPS pulse pattern generator (PPG). To supply the input streams to the MUX, a field programmable gate array (FPGA) platform with four outputs of 10GBPS is available from Xilinx.

To provide a proof of concept test, equipment already available at Montana State University Spectrum Lab was used to demonstrate the generation of a 20GBPS binary bit stream. The equipment in-house includes an ***Inphi*** MUX (2080MX), which produces a 20GBPS stream from four 5GBPS input streams, and two ***Advantest*** PPGs (D3186), which produce bit streams up to 12GBPS. Due to the design of the PPGs, an extra device is required to produce a repeatable bit stream. The PPGs lack the ability to arbitrarily start their code sequence based on an external trigger and only have the ability to synchronize their clocks to a 10MHz reference. The missing piece to complete the system is a device to provide real-time clock correction to the PPGs to align and maintain the synchronization of the pattern streams. This is the primary goal of the device developed in this thesis.

During the development of the synchronization device, the opportunity to add flexibility to the device became obvious. In addition to the proof of concept goal of a repeatable 20GBPS data stream, the device could provide the ability to align devices other than the in-house PPGs, making it a tool useful outside of the proposed project.

Another secondary feature is the ability to provide an adjustable timing offset to the bit stream alignment, delaying the start of either device's pattern with respect to the other. Additional features considered include an output of the constant width pulse stream used by the device's phase/frequency detector (PFD), an adjustable input signal threshold, and magnitude correction of feedback control signal level. A summary of the device performance goals for this work is given in Table 1.

Table 1: Summary of Goals for Alignment Project

Primary	Secondary
Produce a repeatable, programmable 20GBPS binary data stream with sub-picosecond RMS jitter utilizing a 20GBPS ***Inphi*** multiplexer and two ***Advantest*** pulse pattern generators operating at 5GBPS	Allow alignment to devices other than PPGs
	Allow controlled delay offset of pattern start relative to partnered device
	Provide an output of the internal pulse streamed used by the phase frequency detector for alignment
	Provide alignment for all PPG output rates
	Allow adjustment of input threshold detection and feedback signal level

Regarding Off-The-Shelf Solutions

The simplest solution for aligning the PPGs would be to purchase a commercially available unit that performs the task, ideally from ***Advantest*** itself. The D3186 model is a discontinued product and there is not a list of accessories to purchase for the units. In fact, there are no pulse pattern generators in the company's new product line, eliminating the possibility of adapting an accessory for a newer device. Earlier experiments utilizing the PPGs relied on manually synchronizing the data streams. The procedure was to

observe both trigger signals on an oscilloscope while manually increasing and decreasing the bit rate to cause the precession of the data patterns. Once aligned, the bit rates can be set equal to stop the precession. The clocks of the two devices were held aligned by a 10MHz reference. The alignment of the streams would remain for a considerable length of time, but must be realigned after any power reset or pattern length change. The streams also would lose alignment on their own with only the clock being synchronized. To automate this process, the bit rate of one of the PPGs needs to be adjusted smoothly. This feature is not available on our units but can be created by using an external clocking device for one of the PPGs that does have the ability to be adjusted. This approach to alignment is a phase locked loop (PLL) application. Typical commercial PLL units, such as the TLC2933 from ***Texas Instruments***[4], accept as input, the two signals to be aligned and output a voltage controlled oscillator (VCO) signal to clock one of the devices. The output VCO frequency is bound to a range specific to the PLL. The TLC2933 has a VCO range of 64MHz to 96MHz, while accepting input signals up to 30MHz. If the VCO signal was to be used, it would require several multiplication stages to reach 5GHz. PLLs with GHz capable VCOs, such as the ADF4118 from ***Analog Devices***[5], are capable of GHz rates, but limit the input signal frequency from 5MHz to 55MHz. With longer data patterns, the PPG trigger pulses can have repetition rates in the kHz, thus requiring multiplying of the trigger pulse signal frequency.

The unique operating characteristics of the PPGs and the expected data rates of the system make finding a predefined PLL unit difficult. The situation is unique in that the alignment trigger rate is much lower than VCO needed to clock the adjustable bit rate

PPG. Also, there is a wide variance in the trigger rates and the VCO center frequencies needed to align the PPGs across the entire spectrum of pattern lengths and bit rates the device is capable of producing. A custom approach to creating the PLL is a more elegant solution, allowing each portion of the PLL system to be adjusted to meet the SSH-ADC system operating characteristics. The synchronization unit can be built to apply a slow (tens of Hertz) correction to the megahertz trigger pulses, which control the gigahertz data rates. The components to design such a low frequency loop filter are much less expensive than obtaining a commercial unit with a high loop filter bandwidth and operating range.

Design Strategy

A generic system diagram is given in Figure 2 as a project design template. The elements available in-house are the PPGs, the MUX, the radio frequency (RF) signal generator, and the MUX clocking generator. The heart of the alignment system has the form of a PLL, with the PFD providing the error signal, the integration block acting as a low pass filter, and the RF modulated clock acting as the VCO. The PFD and integrator are the pieces of equipment needed to realize the primary goal. The system requires no input signals and directly provides the MUX output. The output signal is a 20GBPS binary data stream made up of the four PPG data and data complement signals, arranged in a predetermined order. Figure 3 displays an example of a 20GBPS data stream created when the MUX inputs are PPG1, $\overline{\text{PPG1}}$, PPG2, and $\overline{\text{PPG2}}$ respectively. The output

stream has the limitation that the code pattern is not completely arbitrary and relies on signal complements to produce the two additional input streams. For the proof of concept, the output data stream patterns need only contain frequency characteristics of a 20GBPS signal and are not required to be fully arbitrary. Use of the PPG data streams' differential pairs ensures the multiplexed stream will have the full spectrum of frequency components. To produce the enhanced feature of arbitrary waveform generation, input streams at 10GBPS are required with the addition of a 2 input to 4 output serial to parallel converter.

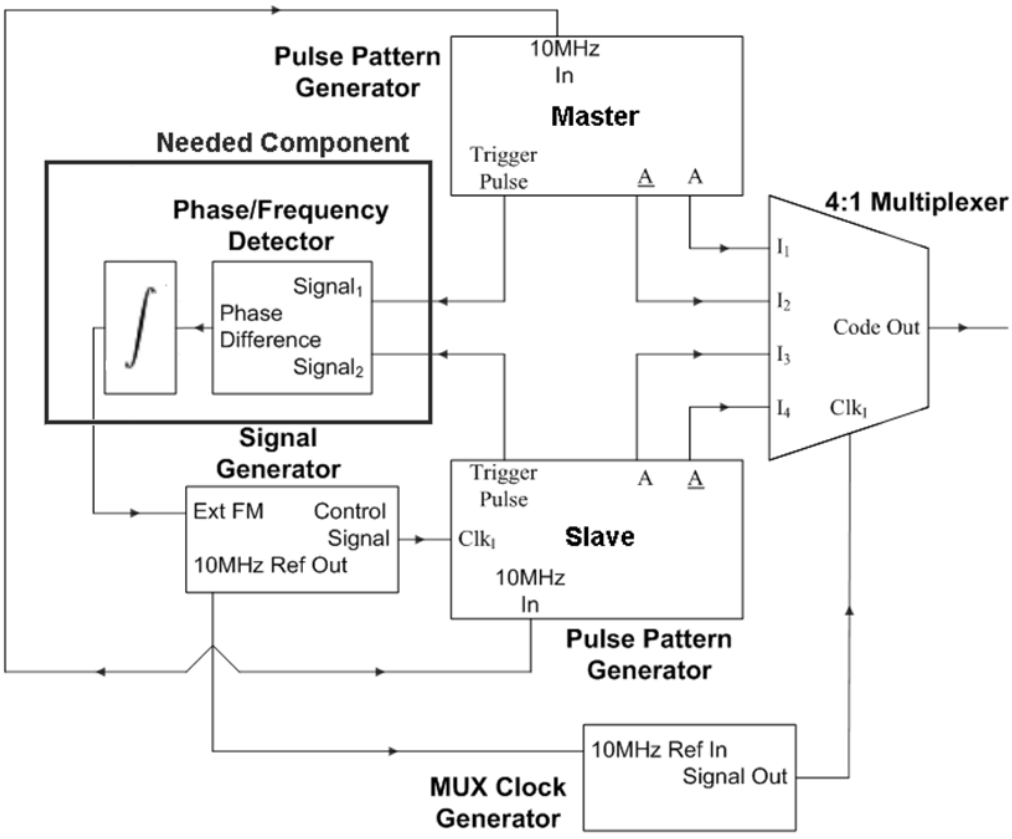


Figure 2: General Block Diagram of Reference Signal System

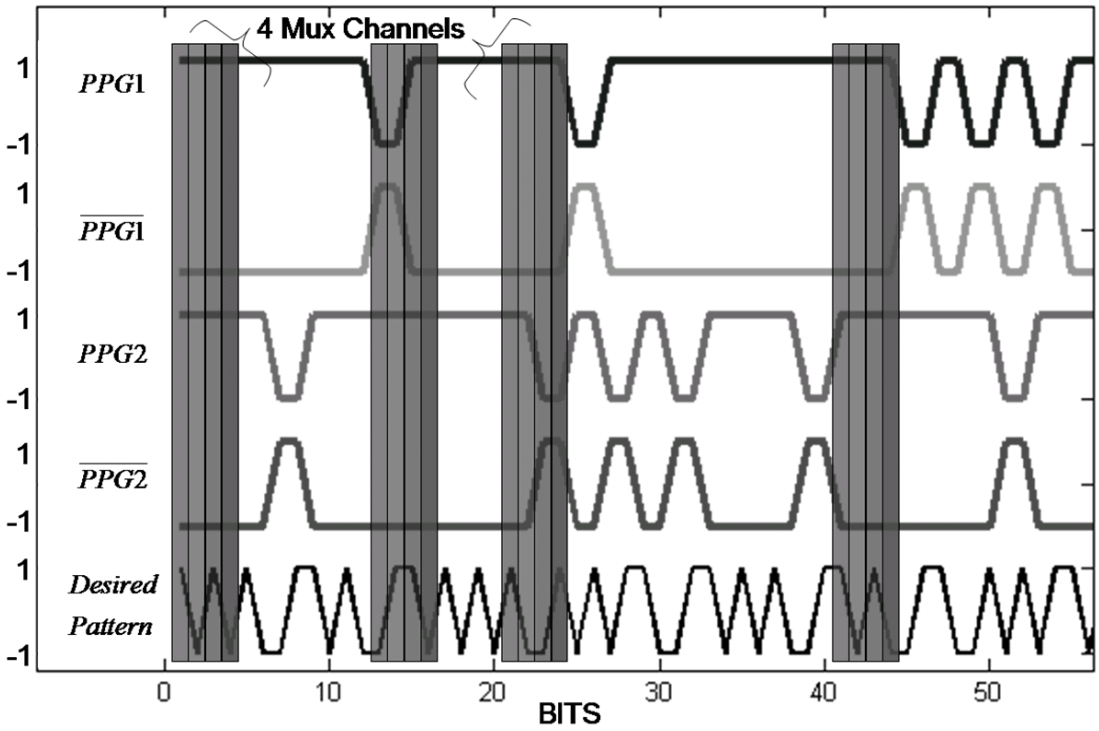


Figure 3: PPG Data Programming for Pattern Generation

To address the need of pattern alignment, the system will make use of the external clocking feature of one PPG, making it a slaved device, as well as both PPGs' output trigger pulses which mark the beginnings of the devices' programmed pattern output. This clock will be provided by an external signal generator which has the ability to frequency modulate the signals generated. This signal can then be used to adjust the PPG operating rate, allowing for the pattern start point to be temporally translated with respect to a reference point. The reference point will be provided by the master PPG operating with an internal clock. The end result of the modulation will be the precession of the pattern start trigger of the slave device relative to the master PPG. The modulation signal provided to the generator providing the slave clock will be directly related to the temporal difference of the master and slave pattern triggers. The device to be designed will need

to incorporate a phase/frequency device to provide the modulation control signal. Additional 10MHz clock synchronization signals will be used to align the MUX clock with the PPG clocks.

Use of the device to feedback the real time temporal difference of the pattern triggers in the form of a control signal allows this system to automatically adjust and maintain pattern alignment.

Complementary Code Design

While the production of the 20GBPS data stream is the primary concern of the project system, the nature of the reference code pattern is important and must be considered if the 20GBPS stream is to have the required spectral characteristics in the proposed digitization method. Specifically, the reference codes chosen must be complementary sequences. Skolnik[6] defines complementary sequences as follows.

> Complementary sequences consist of two sequences of the same length N whose aperiodic autocorrelation functions have sidelobes equal in magnitude but opposite in sign. The sum of the two autocorrelation functions has a peak of 2N and a sidelobe of zero…In a practical application the two sequences must be separated in time, frequency, or polarization…

Figure 4 gives the spectra of two codes that are complementary. Notice when added, the side bands cancel and only the primary component remains. Since only two 5GBPS data streams are available, the four bit inputs to the MUX must be in the form of a seed term able to create complementary sequences. (1, 1, 1, 0) and (1, 1, 0, 1) are a

complementary seed pair that meet this requirement. These seeds were determined using the ***Matlab*** script located in Appendix C. To create this, the PPG data streams need to be applied as (PPG1, PPG1, PPG2, $\overline{\text{PPG2}}$) to the MUX.

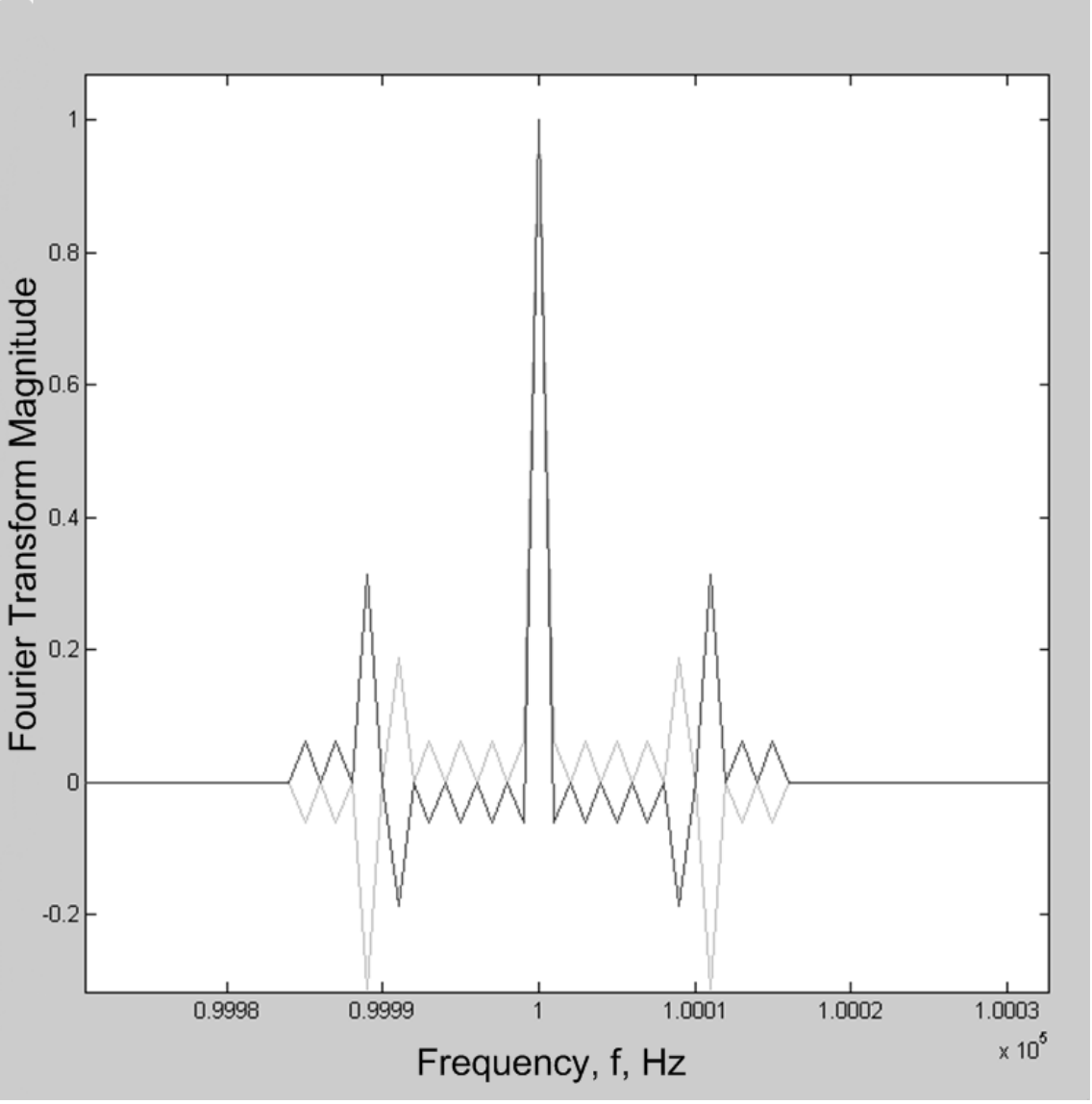


Figure 4: Example Spectra of a Complementary Pair

Table 2 gives the resulting four bit combinations provided by the MUX output stream while Table 3 gives the timing diagram of the 20GBPS signal compared to the PPG input streams. The sampling architecture of the MUX forces the PPG input values to be delayed by one 5GHz clock cycle before being inserted in the output stream.

Table 2: Possible Bit Sequences Using the {1 1 1 0} Seed

PPG 1	PPG 2	Multiplexed Sequence
0	0	0001
0	1	0010
1	0	1101
1	1	1110

Table 3: Timing Diagram for 20GBPS Complementary Sequence Code Generation

MUX Clock (20GHz)	1	0	1	0	1	0	1	0	1	0	1	0
PPG Clock (5GHz)	1				0				1			
PPG1	1				1				0			
PPG1	1				1				0			
PPG2	1				0				0			
PPG2	0				1				1			
MUX Output	X	X	X	X	1	1	1	0	1	1	0	1

Use of a specific 4 bit seed sequence of (1, 1, 1, 0) allows the produced 20GBPS stream to be the complementary sequences required for the reference signal in the SSH-ADC operation.

SYSTEM EQUIPMENT SPECIFICATIONS

As the primary goal of the synchronization device is to operate on in-house equipment, the equipment characteristics are necessary to the device design. The following offers a brief description of the item available as well as several key specifications.

Advantest D3186 Pulse Pattern Generator

The Advantest PPG[7] is used to provide programmable binary data streams at rates between 150MBPS and 12GBPS from either internal or external clocking. The PPG's memory can accommodate code lengths up to 8,388,608 (2^{23}) bits programmed through a GPIB interface. The data stream is available as a differential pair through two SMA connectors. The voltage of the output stream can be set from $0.5V_{pp}$ to $2V_{pp}$ with the absolute range confined to +/-2 volts. Rise/fall times are less than 30ps with a root mean square (RMS) jitter less than 1.5ps.

Other outputs available include the internal clock in differential form as well as ½ and ¼ clock rate signals, a 10MHz reference signal is both produced and accepted as an input, and a trigger signal operating at 1/32 of the master clock or as a marker pulse for data pattern beginning.

The trigger signal of interest for device alignment is the pattern start pulse. This pulse has different characteristics depending on the length of the data pattern and the bit rate of operation. Equation 1 specifies the repetition rate for the pattern trigger.[9]

$$\boldsymbol{R} = \{\boldsymbol{LCM}(\boldsymbol{PL}, 256)\} * \frac{\boldsymbol{N}}{\boldsymbol{clock}} \quad (1)$$

In the equation LCM(PL, 256) is the least common multiple of the pattern length (PL) and 256 bits. This term arises from the PPG's inability to produce a trigger pulse with high repetition rates. The base trigger pulse the PPG produces is for a code of pattern length 256. Thus if the pattern length is 3, 3 blocks of 256 are needed for the pattern trigger to continually occur at the 3-bit pattern beginning. N in this expression is the binary exponent to one more than the pattern length ($PL+1=2^N$) and clock is the master clock frequency in Hz. As an example, consider a pattern length of 3 (2^2-1) at a bit rate of 12GBPS. Using equation 1, a pulse separation of 128ns is obtained. This pulse separation leads to a repetition frequency of 7.8MHz.

The width of the trigger pulse is given by equation 2.[10]:

$$\boldsymbol{PW} = \frac{32}{\boldsymbol{clock}} \quad (2)$$

For a 12GBPS bit rate, the pulse width would be $2.67*10^{-9}$s or 2.67ns. While the repetition rate for the pulses is relatively low, a pulse width of this width requires very sharp rise and fall times. Good quality SMA cables with low attenuations below 20GHz will keep the pulse edges sharp. Minimum pulse width requirements of off-the-shelf devices often limit use of the PPG trigger pulses for high precision pattern alignment.

Maxim MAX9382 Phase/Frequency Detector

The initial phase/frequency detector purchased for the system is a discrete chip mounted on an evaluation board from ***Maxim***[11]. This detector compares two single-

ended, ECL/PECL input signals, the reference signal (R) and the voltage controlled oscillator signal (V). The PFD produces differential up (U) and down (D) pulse output streams governed by the input signal phase difference. The output pulses have a minimum width of 450ps. Figure 5 shows the relation between the output signal's and the input signal's phase difference[12]. An integration circuit uses the difference of the PFD U and D signals as its input to provide the control voltage for the device producing signal V. The chip is designed to have a maximum operating frequency of 400MHz. The U and D signals have a maximum delay relative to the input signals of 60ps and an added RMS jitter of 1ps.

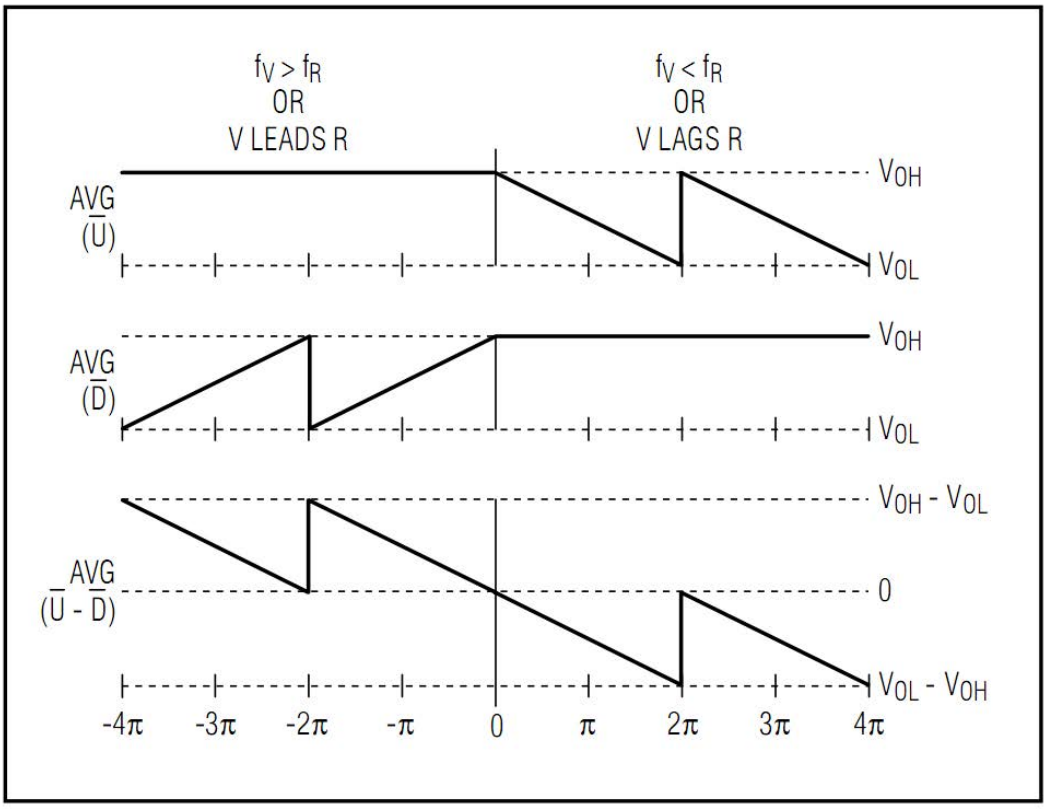


Figure 5: PFD Output Voltage vs. Input Phase Difference

Agilent E4432B Radio Frequency Signal Generator

The ***Agilent*** E4432B[13] is the only in-house device available for producing a frequency modulated clock signal used to externally clock the slave PPG. The frequency modulation can be controlled by an external input with a signal range between +/- 5 volts. The generator allows for modulation deviations up to 100kHz, dependant on a manually controlled deviation constant. Since the maximum generated signal is limited to 3GHz, an in-line frequency multiplier unit is required to achieve the necessary 5GHz clock signal. Additional multiplier units would be needed to provide full PPG functionality at 12GBPS. The output power of the E4432B peaks at 10dBm for the 1GHz to 3GHz frequency range. The RMS jitter of the output signal is listed to be no greater than 100fs.

Inphi 2080MX 20GBPS 4:1 Multiplexer

The ***Inphi*** multiplexer[14] is the key device in the production of the high bit rate signals. The device operating characteristics are the primary determinants of the bit rate, rise/fall times, and RMS jitter of 20GBPS data stream. Figure 6 gives the timing information for the MUX. The device operates with a 20GHz externally supplied clock and four data input lanes, providing the 20GBPS output and a 5GHz clock. The input channels are limited to $1V_{pp}$ single ended. The MUX samples the four parallel data lanes and then produces the serial data stream one clock cycle after the sampling period. The output stream is differentially $1V_{pp}$, with rise/fall times of 12ps and RMS jitter of 500fs. The output clock has similar voltage levels and jitter, but rise/fall times of 25ps.

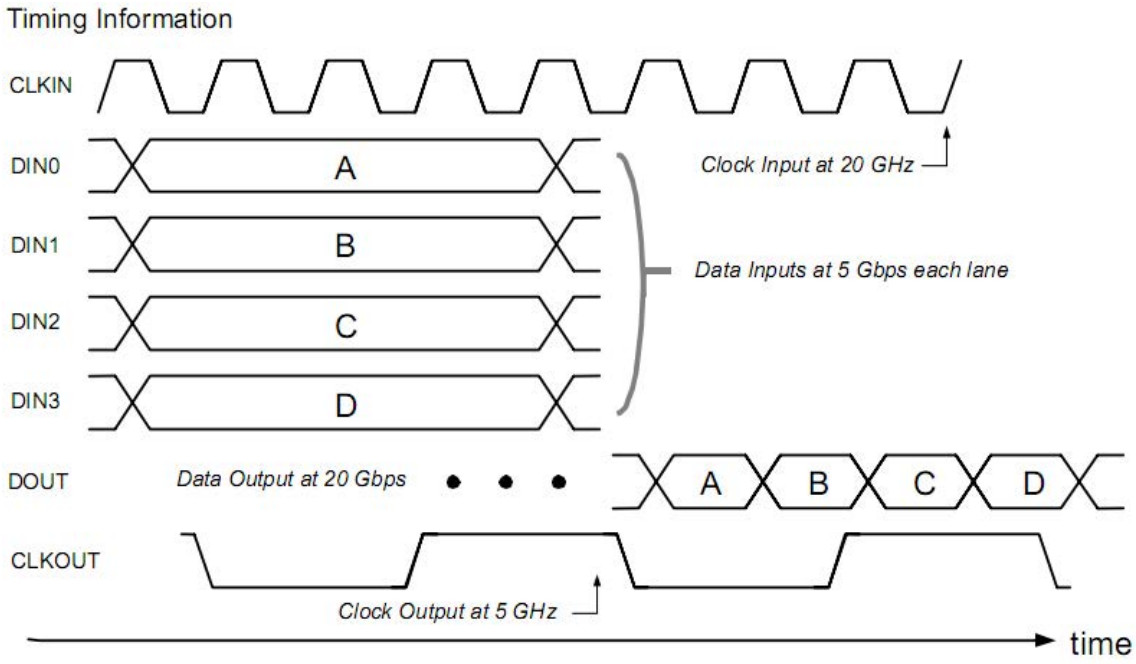


Figure 6: ***Inphi*** 2080MX Timing Diagram[15]

Agilent 83752A 20GHz Sweep Generator

The ***Agilent*** 83752A[16] is the in-house device available to produce the 20GHz clock signal for the MUX and can be used as the slave PPG clock when operated at 12GBPS. The output signal of the generator has a power range of -15dBm to 17dBm and a specified RMS jitter of 1.4ps. A 10MHz signal input is also available for clock synchronization.

CIRCUIT IMPLEMENTATION

SSH-ADC Reference Generator as a Control System

The general block diagram of Figure 2 can be broken down into a general control system which is shown in Figure 7. This has the general form of a phase locked loop.[17]

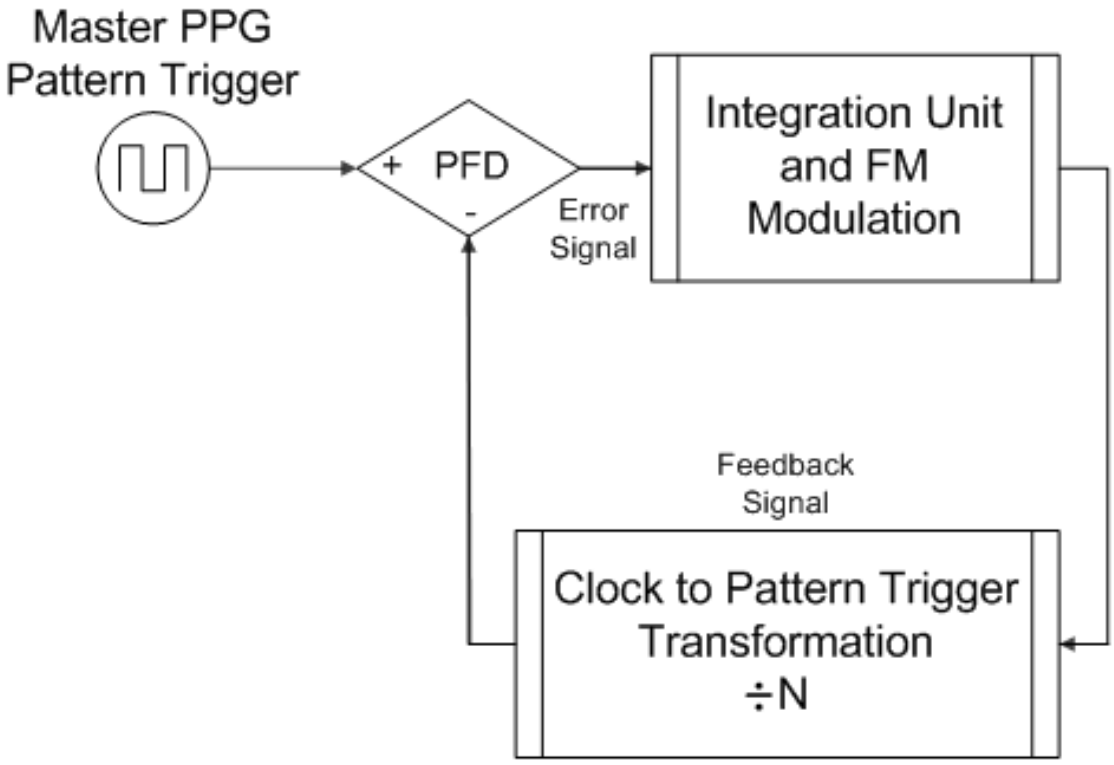


Figure 7: Overall Control System Model

The phase error between the PPG trigger signals is the error signal for the control loop, which is fed into the integration circuit. The control system consists of the integration circuit up to the FM modulator of the slave PPG's clock generator. The feedback term of the control loop consists of the electronics which convert that

modulation signal into the pattern trigger of the slave PPG. This approach uses the MHz trigger signal to align the much higher frequency 5GBPS data streams. The ***Maxim*** PFD chosen for this project operates at a maximum of 450MHz and is the fastest such device offered by the company. With this upper operating limit, the PFD would not be sufficient if it operated directly on the data streams. While the system acts as a phase locked loop, it is locking the phase of the slower pattern trigger rather than the faster PPG clock. Further, the precision of the clock devices involved, allows for relatively long periods of time to pass before disturbance correction must be applied. This allows the integrator to operate like a low pass filter with a low corner frequency. With this low corner frequency, a simpler integrator design is needed without requiring high performance ICs to maintain stability. In this way, an inexpensive, low bandwidth phase lock loop system controls very high data rate components, aligning them to produce data streams capable of being multiplexed to a rate of 20GBPS. Choosing the appropriate bandwidth for the integration circuit will be addressed in a separate section.

Circuit Operation Overview

To address the challenge of PPG synchronization, the Periodic Event Synchronization Unit (PESU) was developed to provide automated, real-time correction to the pattern alignment. Figure 8 provides a general functional overview of the PESU. The device does this by providing the control signal based on the difference between the two periodic event signals, the PPG pattern triggers. The PESU was designed to convert the input event pulses into a constant width pulse trains which meet the phase detector's

minimum pulse width requirement. The up/down PFD signals are integrated to provide an accumulation of the amount of error between the event pulses of the devices to be aligned. This integrated signal is the output from the PESU and is connected to the frequency modulation input of the slave PPG's external clock. As the phase difference between the two periodic events changes polarity, the integrator signal adjusts to precess the slaved device trigger in the other direction. This process causes active alignment of the periodic triggers to a minimum offset error oscillation.

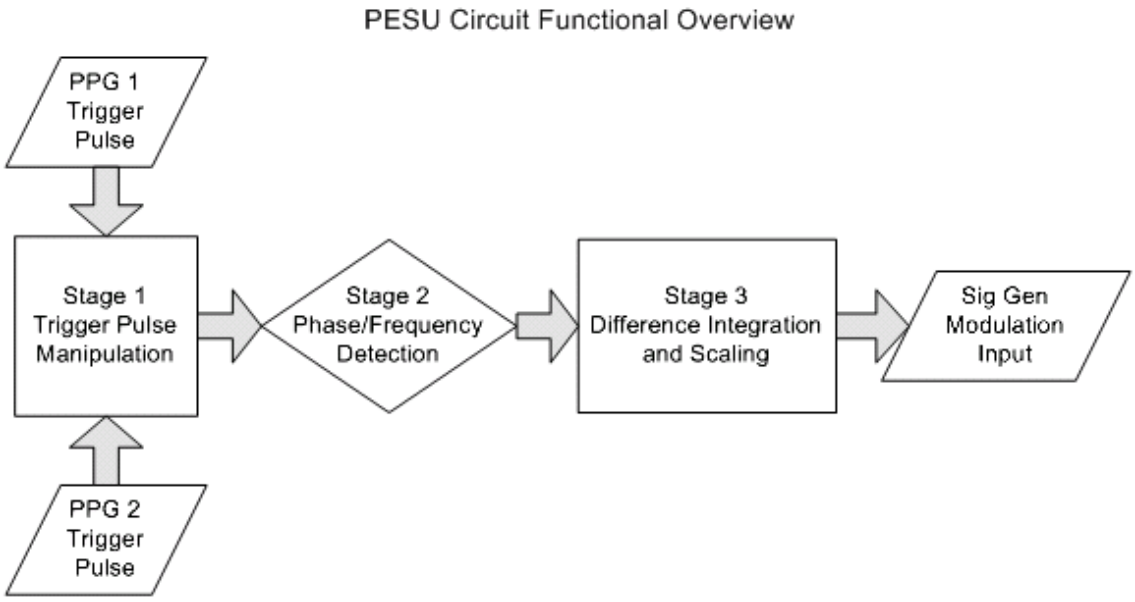


Figure 8: Block Model of Signal Stages in PESU

While the design of the PESU was tailored to operate with the PPG pattern triggers as the periodic event inputs, the alignment functionality can be applied to other devices, as long as two periodic event pulses are present and one of the event pulses can be adjusted by frequency modulating a device clock signal, either internally or externally.

Using multiple PESUs will allow one master signal to align several devices. Devices that feature an external trigger option do not need the PESU for alignment; however custom made devices often lack an external trigger.

Synchronization device operation is broken up into three stages, producing the required control signal from the event signals. The three stages include event pulse modification, event pulse phase detection, and control signal generation. The initial synchronization device was designed to only accomplish the primary task. After the initial circuit was prototyped, several flaws in the design became apparent as well as opportunities to add functionality. Care was taken in the redesign of these stages to provide additional abilities to the PESU beyond the primary PPG trigger alignment task. Additional features include indifference to input event signal form, introduction of temporal event offsets, creation of an output corresponding directly to the reference event signal, up/down differential magnitude correction, and reduction of errors in integration.

The specifications of the in-house equipment provided the primary design criterion for the PESU. Of primary concern were the pattern trigger signal specifications for the two PPGs and the modulation input requirements of the 3GHz external clocking source. The most difficult task was the transformation of the pattern triggers into a form suitable for the PFD, which was addressed in the first stage. The modulation input requirements of the 3GHz clock were easily achieved, but gain control of the output signal was necessary to adjust the control loop constants for performance optimization. The two performance considerations to be optimized were the response time of the control loop to misalignment of the trigger events and the amount of steady state error

that exists once the triggers were aligned. Faster alignment response comes at the cost of increased steady state error. Keeping steady state error from introducing significant bit misalignment was crucial to the correct operation of the MUX as large errors cause repeated output pattern changes. Fast alignment response is not as critical due to the exceptional frequency stability of the PPG internal clock and the signal generator. Faster response times are desirable when increases in PPG pattern lengths decrease the event trigger frequencies to hundreds of kHz, as larger amounts of error accumulate between each event signal phase comparison.

PESU Circuit Stage 1: Trigger Pulse Manipulation

The first stage of the PESU addresses the need to change the shape and duration of the trigger pulse so that the PFD can function optimally. Figure 9 displays the circuit schematic for the first revision of the PESU. Initially, the trigger pulses were transformed into clock signals by using the trigger signals to clock D-flip-flops (DFFs), parts U2A and U2B. This method produced two square waves at half the frequency of the pulses on which the PFD operated. Since the triggers are so brief, it was necessary to extend them in order for the DFF to clock properly. The combination of the capacitor, resistors, diode and transistor at the trigger input serves to lengthen the pulse. The pulse travels through the capacitor first which blocks the DC component of the signal. This forces the pulse to a positive voltage. A diode is used to engage or disengage the transistor amplifier. If the trigger signal is negative in voltage, the diode acts to bypass the resistor in parallel to it, which provides a very low resistance path to ground for the

base terminal. When the pulse occurs, the signal is driven positive and eventually closes the path to ground through the diode. This enables the transistor to act in amplification. The slower nature of the transistor extends the trigger pulse to a length which can clock the DFF. Adding a variable resistor to the parallel diode path of the modulated trigger signal allows the operator to adjust at what level the transistor acts. This is used to delay the clocking of that path's DFF which can be used to compensate for any timing issues between pattern data and the trigger pulse.

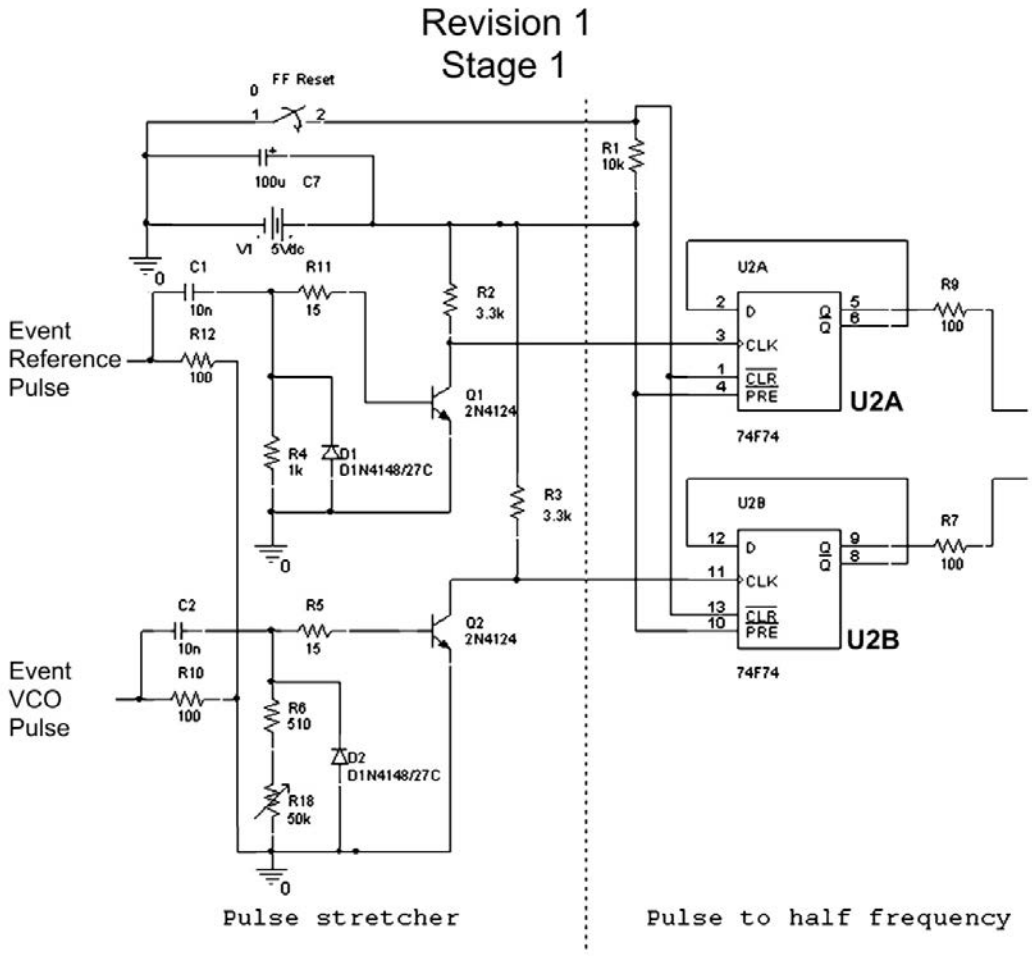


Figure 9: Stage 1 Schematic Revision 1

While the prototype correctly aligned the PPG data streams, enhancements to the design allowed for lower alignment error and added functionality to the PESU. Figure 10 displays the second revision to the PESU board.

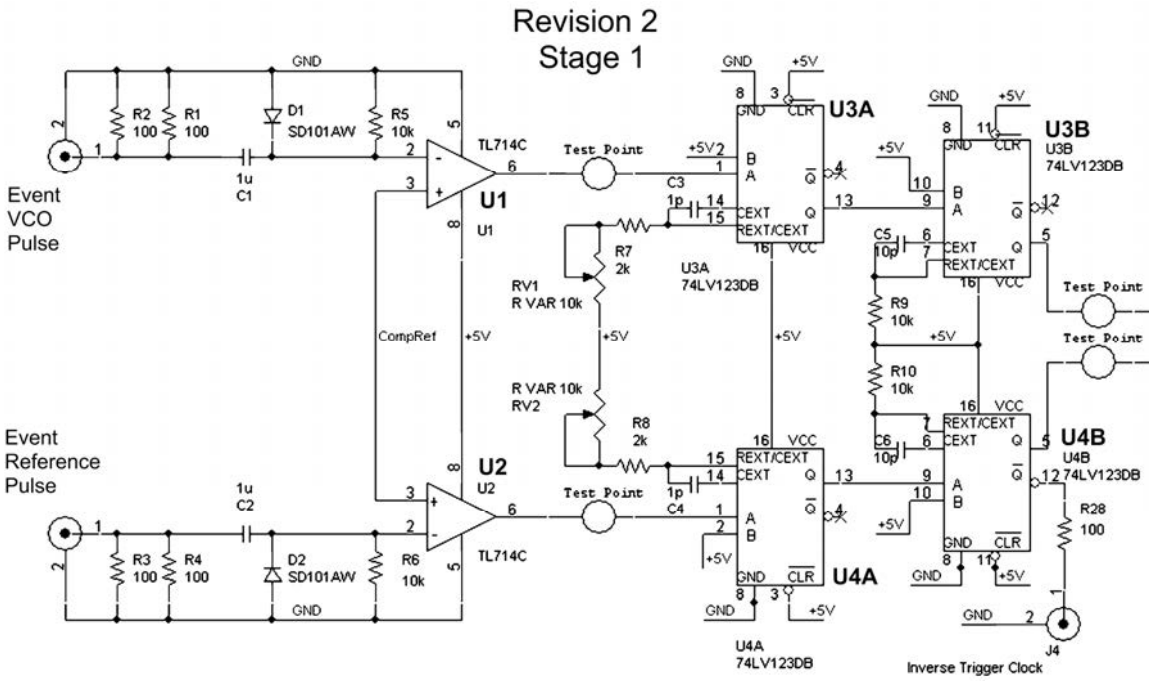


Figure 10: Stage 1 Schematic Revision 2

Figure 11 shows the ideal transformation of event pulses by the second revision circuit. By replacing the transistors with comparator ICs (parts U1 and U2) the transformed pulse can be triggered by an independently set reference voltage. This provides a more accurately defined pulse edge for the extended trigger pulse. Making the reference voltage variable also allows for the optimizing of the comparator operation to triggers of different shapes and amplitudes. The comparators create pulses with similar shapes and uniform amplitude, even if the input signals have very different characteristics. Thus the devices to be aligned are not limited to being identical in trigger

signal characteristics. Replacing the DFF with two retriggerable monostable multivibrators (RMMs) ICs (parts U3A, U3B, U4A, and U4B) adds increased functionality to the PESU. The RMMs allow a variable pulse width signal to be created from the falling edge of an input pulse. By placing two RMMs in series, the timing of the final output pulse can be dictated by the width of the pulse created by the first RMM. This first RMM features a variable resistor in the pulse width control path to allow real time adjustment of the intermediate pulse's width. By placing this arrangement of RMMs in both the reference and modulated signal paths, either signal can be delayed with respect to the other. This increases the ability of the PESU to compensate for any misalignments of the trigger signal to the pattern data. In the case of synchronizing two PPGs, the arrangement allows the data pattern to be shifted to the optimal alignment for the multiplexer. The width of the pulse of the second RMM is set to meet the PFD input requirements.

Figure 12 displays the possible pulse widths available to the RMM[18]. The PFD requires a minimum of 450ps of pulse width for operation, which all the configurations of R_{EXT} and C_{EXT} meet. Values of 10kΩ and 10pF were chosen to produce a 200ns pulse width. For the first RMM, a 1pF capacitor is used to allow for the smallest possible pulse width. The resistance is set to vary between 2 and 12kΩ, which corresponds to a pulse width range of roughly 50ns. Adjustability in both paths allows the modulated pattern trigger to lead or lag the reference trigger by 50ns. A 50ns pulse width corresponds to 250 bits in the PPG data stream.

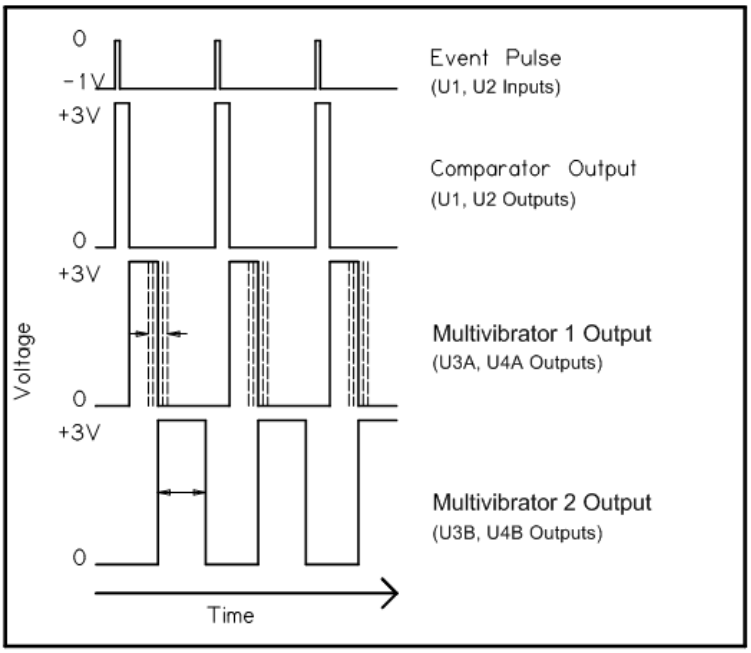


Figure 11: Ideal Event Pulse Manipulation

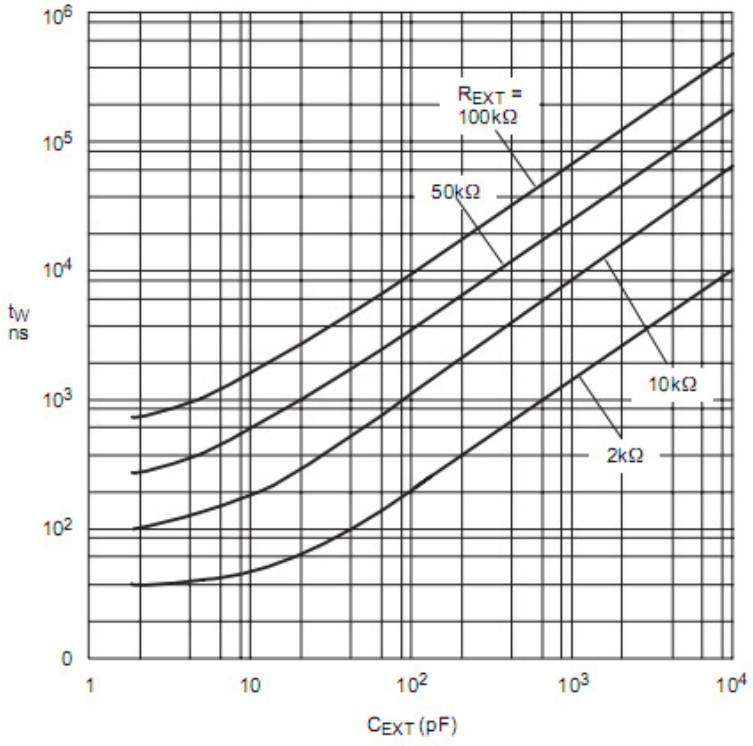


Figure 12: RMM Output Pulse Width for External Resistor/Capacitor Combinations

PESU Circuit Stage 2: Phase/Frequency Detection

The second stage of the PESU is the implementation of the PFD IC as shown in Figure 13. For the prototype, the PFD was mounted on an evaluation circuit board. The evaluation board operated using 2 voltages, -3 volts and +2 volts. This combination of voltages allowed the PFD output to range from approximately 0 volt to 1 volt ideally. The prototype utilized the U and D outputs in a single ended fashion. Figure 14 gives an example of the U and D waveforms for both a positive and negative phase difference between the reference and modulated signal[19]. U and D mirror each other in pattern, depending on the sign of the phase difference.

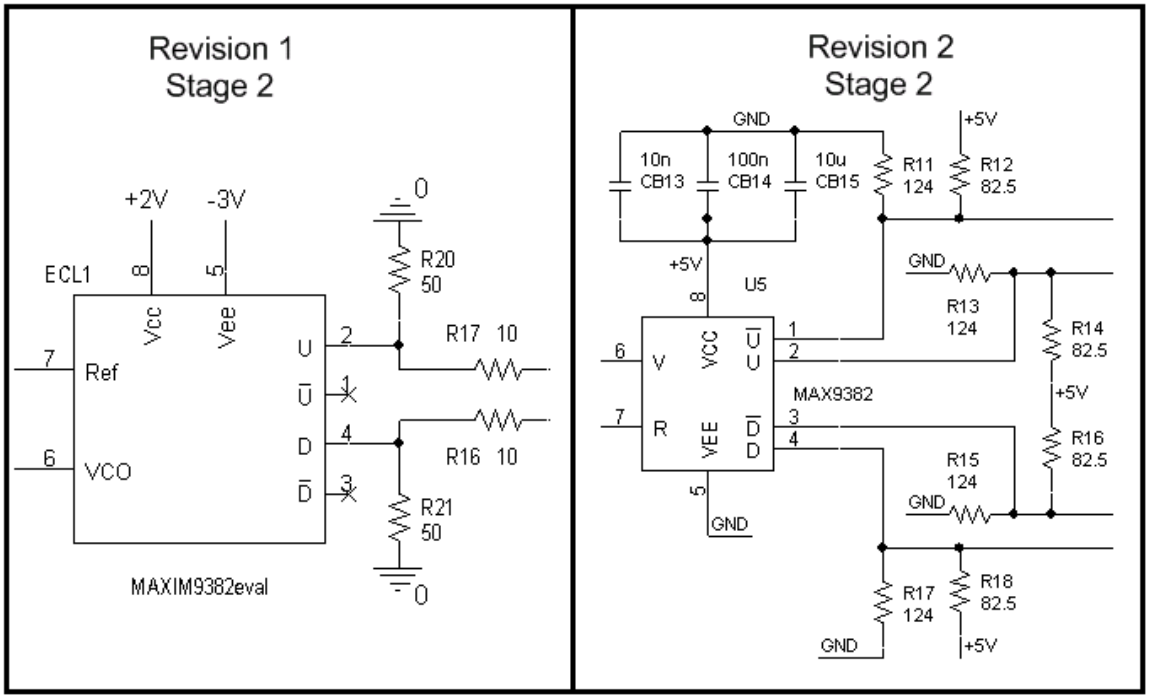
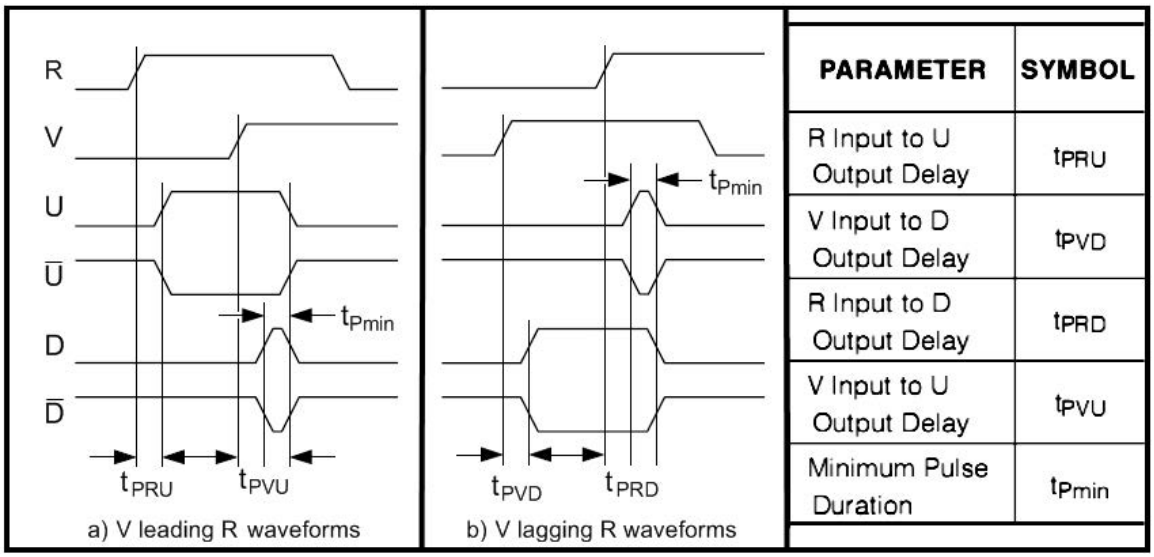


Figure 13: Stage 2 Schematics (Revision 1 left and Revision 2 right)



PARAMETER	SYMBOL
R Input to U Output Delay	t_{PRU}
V Input to D Output Delay	t_{PVD}
R Input to D Output Delay	t_{PRD}
V Input to U Output Delay	t_{PVU}
Minimum Pulse Duration	t_{Pmin}

Figure 14: Ideal Response of PFD to Similar Frequency Inputs

The revised circuit removes the need of the evaluation board and positions the PFD IC directly on the PESU circuit board. There were several drawbacks to using the evaluation board as a standalone phase detector. The board is designed to operate so that the output signal has a low near ground, which entails operating at -3 volts and +2 volts. Since none of the other ICs in the design operate with these voltages, 2 additional voltage regulators or supplies are required. Another complication of the evaluation board is the interfacing required between stages. The board expected signals to enter and exit the board via coaxial cables with SMA type connectors. The initial design avoided this by sending signals to the board by soldered bridging wires. When moved to the main PESU circuit board, the operating voltage of the PFD was changed to ground and 5 volts to reduce the number of power voltages. This change in voltage changes the signal levels of U and D to operate with highs near 4 volts and lows slightly over 3 volts. To match the input requirements of the next stage, the impedance matching resistors of the U and D

signals were changed to a bridge configuration between ground and 5 volts. The choice of 82.5Ω and 124Ω resistors allows the bridge to keep the 50Ω impedance to AC signals.

PESU Circuit Stage 3: Difference Integration and Scaling

The first revision of the final stage of the PESU is given in Figure 15. The first iteration utilizes a simple difference integration circuit featuring a +/-15 volt operational amplifier and driven by the single ended U and D signals from Stage 2. Resistor and capacitor values in the integrator were chosen to optimize the integrator operation to several MHz. A voltage divider is used before the PESU output to allow for adjustment of the integration magnitude. This adjustment allows the control loop gain to be adjusted to optimize for steady state error and response time over a range of pattern trigger repetition rates.

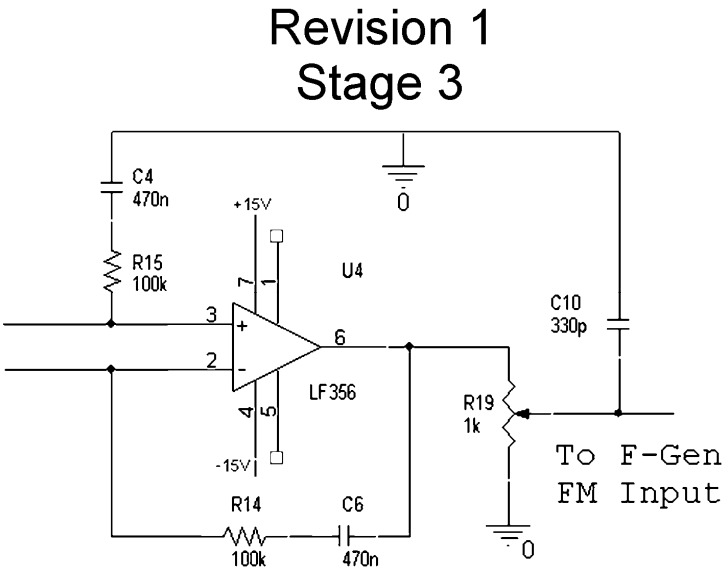


Figure 15: Stage 3 Schematic for Revision 1

The second revision keeps the difference integration circuit but with several changes and is shown in Figure 16.

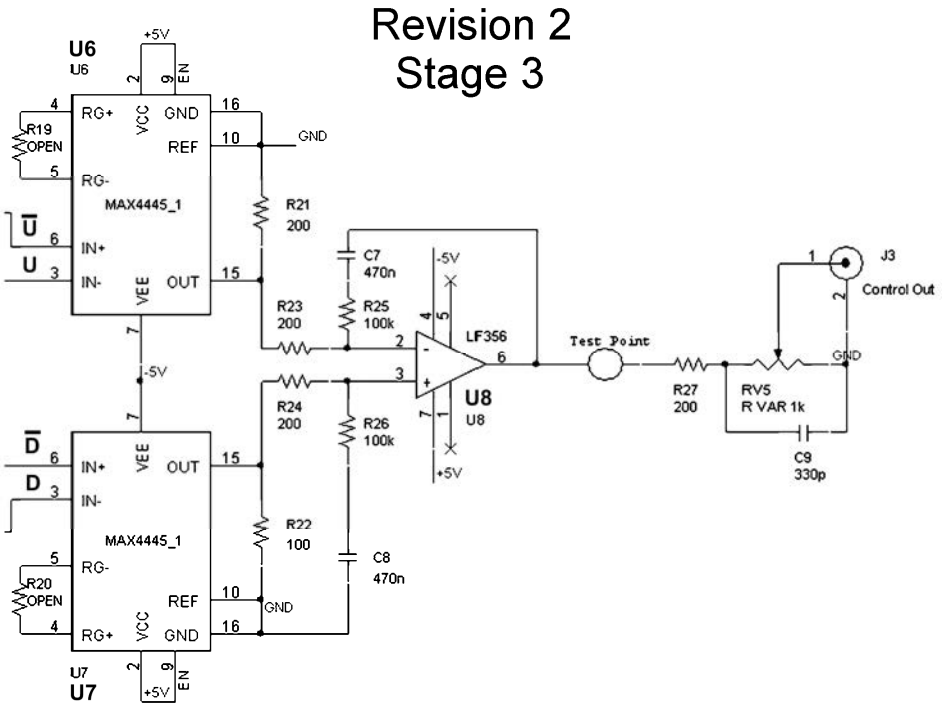


Figure 16: Stage 3 Schematic for Revision 2

First, the operational amplifier was changed to operate at +/-5 volts, to match the other ICs on the board. Second, the input to the difference integrator changes from the singled ended U and D signals to (U- $\overline{U}$) and (D- $\overline{D}$). Idealized voltage traces of the PFD inputs and outputs as well as the PESU control signal are given in Figure 17. The differential U and D signals are transformed to signal ended signals by a differential amplifier with unity amplification (MAX4445). This change addresses an issue of error in the U and D signals. The voltages applied to the PFD need to be adjusted to specific levels for the U and D signals to be identical to each other. Without this voltage

adjustment, an error accumulates in the integrator as the PESU waits for the next trigger pulses; i.e. the control signal does not have the zero slope regions. The effect is a larger cyclical error in the edge position of the reference trigger as the FM modulation signal never reaches a steady state value and must be corrected at every trigger pulse. By using the MAX4445, the singled ended signals fed to the integrator are the magnitude of the difference between the differential outputs of the PFD. The equality between the (U- $\overline{U}$) and (D- $\overline{D}$) signals is more stable given varying values of applied voltage to the PFD, thus allowing for less error to accumulate due to systematic voltage differences. The voltage supplies to the PFD can now be fixed to +5 volts and ground as there is no error due to differences in U and D. The MAX4445 also features the ability to apply amplification to the signal ended signals from the U and D differentials. This can be used to fine tune the system if there is any error between the (U- $\overline{U}$) and the (D- $\overline{D}$) paths due to component variability. This amplification is adjusted by adjusting the resistance between the RG+ and RG- pins of the MAX4445 device.

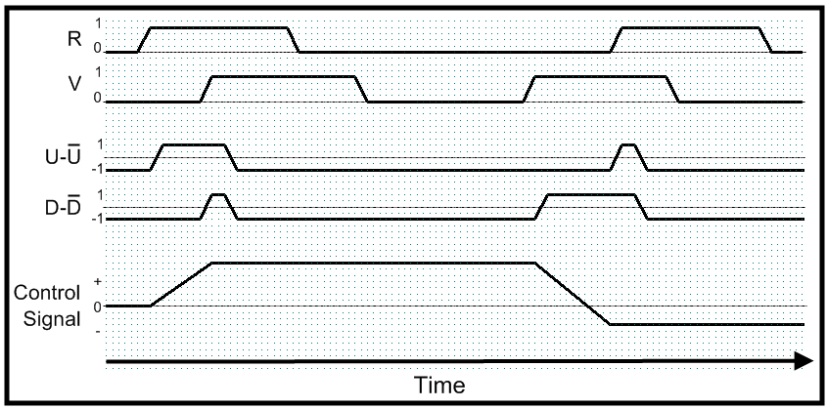


Figure 17: Ideal Integration of PFD Outputs

Integrator Design in terms of the Phase Locked Loop

In designing the third stage of the PESU, pole considerations were determined by the forward transfer function of the PLL. The combination of the integrator and FM unit in the slave PPG clock signal generator are this transfer function. The clock to pattern trigger conversion, which is the feedback function, occurs in the slave PPG. With the signal generator acting as the voltage controlled oscillator (VCO), the PESU third stage forms the loop filter. The integration circuit is an active filter[20] and has the general form of that given in Figure 18. The true integration circuit is a difference integrator, so the controlling resistors and capacitors are repeated on the positive amplifier input with R2 and C going to ground rather than the amplifier output to form feedback.

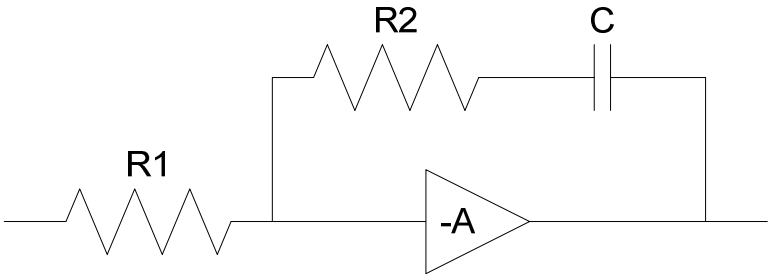


Figure 18: Active Filter Base for Stage 3

The PESU PLL is needed to maintain a reference frequency with no phase error. According to Motorola application note AN535[21], this is a type two system with zero step position and zero step velocity. The loop transfer function given for this system type is equation 3.[22]

$$G(s)H(s) = \frac{(s+a)k}{s^2} \tag{3}$$

G(s) is the forward function and H(s) is the feedback function. In our application, H(s) is a frequency divider which applies a constant value to the loop transfer function. The FM of the signal generator contributes equation 4 to the transfer function.[20]

$$K_o = \frac{K_V}{s} \tag{4}$$

The K_V term is another constant with the s dependence adding an integration term. This leaves the loop filter to have the form of equation 5.[20]

$$K_o = \frac{K(s+a)}{s} \tag{5}$$

The non-ideal nature of the operational amplifier sets a maximum possible gain as well as a maximum voltage it can output. From the form of the active filter, the corner frequency of the low pass filter is determined by the feedback components. From inspection, at high frequencies, the active filter gain will approach (-R2/R1) with the capacitor acting as a short while at low frequencies, the capacitor acts as an open circuit, causing the gain to approach infinity, ideally. The -3dB frequency is given by equation 6.[20]

$$f_{-3dB} = \frac{1}{2\ R_2 C} \tag{6}$$

A ***MathCAD*** script was developed to evaluate resistor and capacitor combinations and is given in Appendix D. The terms in this script have the various constants of the system included. The closed loop response for the selected design parameters is shown in Figure 19 with a -3dB frequency of 48Hz.

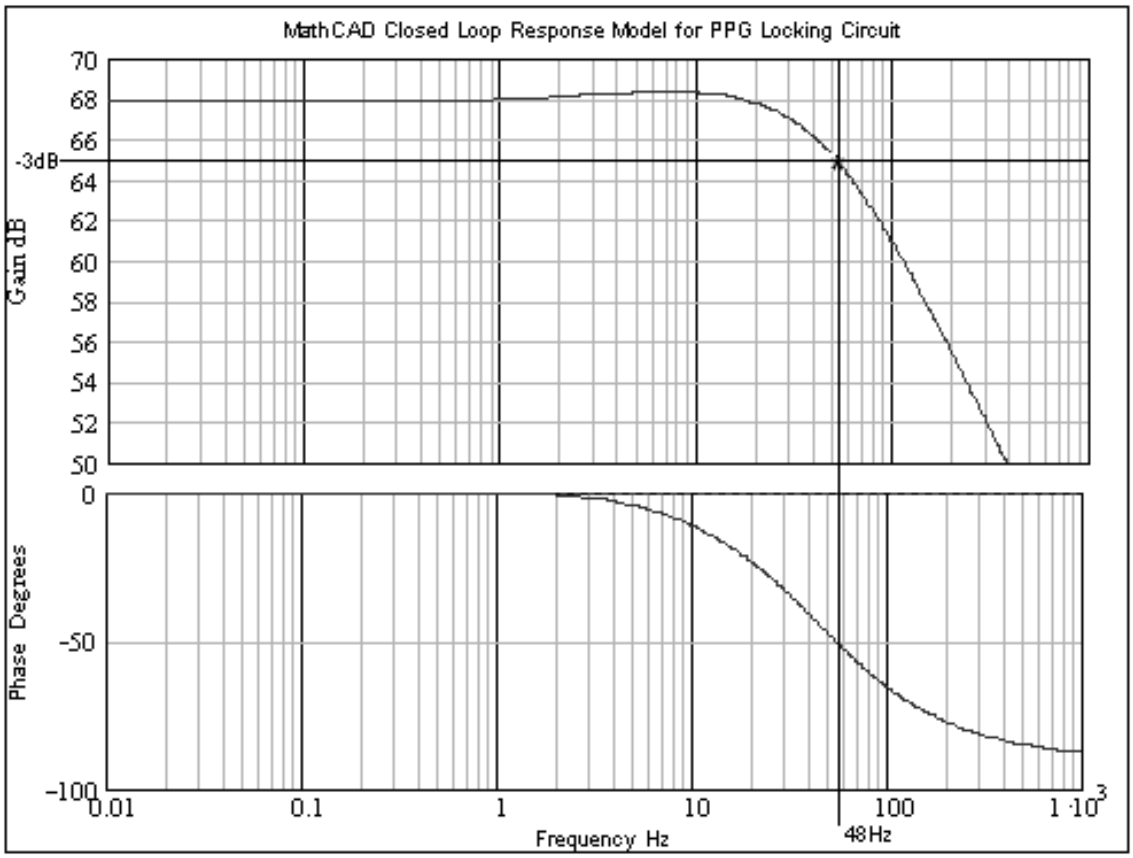


Figure 19: PLL System Closed Loop Bode Plot

Device Fabrication

Figure 20 displays the prototype of the PESU using the revision 1 circuitry. Leaded components and ICs with the dual in-line package (DIP) interface were used with manually routed, copper-clad prototype boards. Besides the traces on the board, jumper wire is used to provide interconnects, including interconnects between each circuit stage. The prototype board is mounted inside an aluminum box with external power, input, and output connections. The prototype provided the basic proof of concept for the PESU and

is robust enough for multiple component/trace changes. The interface is not user friendly and does not have great stability, but was sufficient for an initial proof of concept.

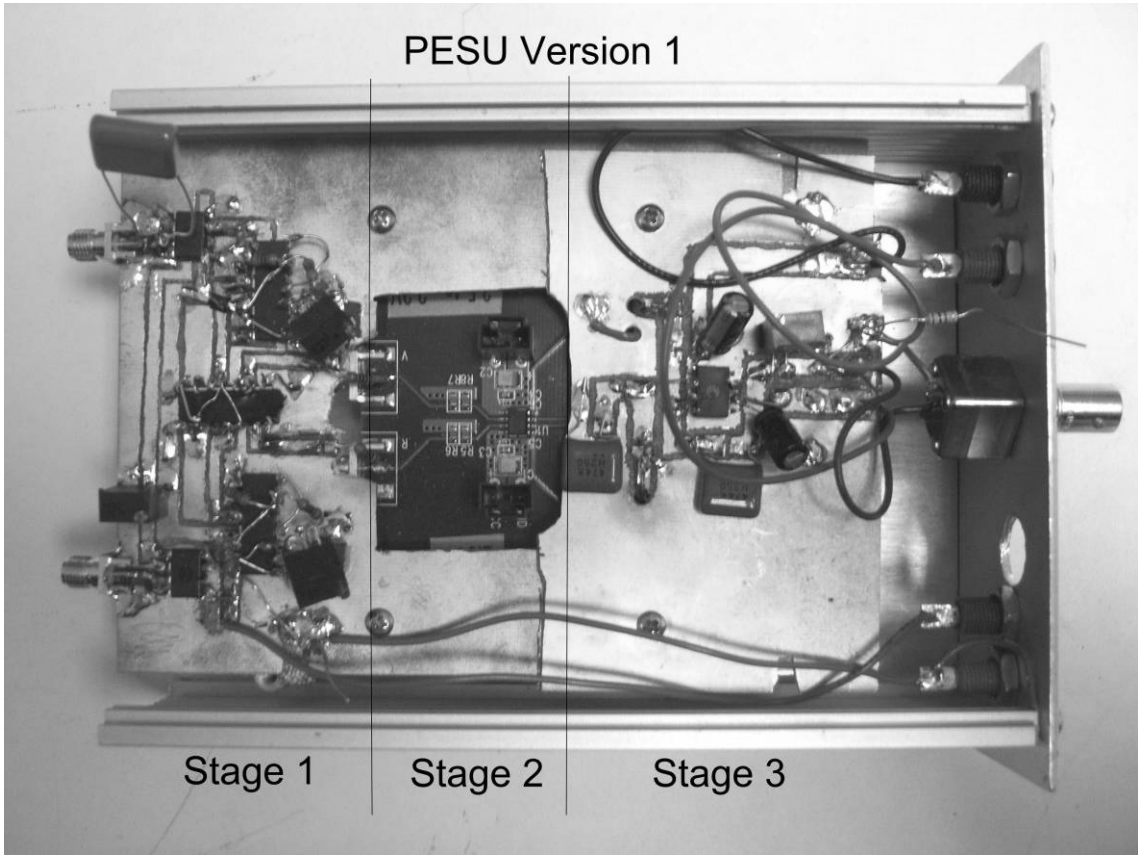


Figure 20: Prototype of Revision 1 PESU

To improve performance, a circuit board was laid out and fabricated for the second revision as shown in Figure 21. The silk screen on the PCB is clearly marked in Appendix B. While the circuit schematic was done with ***Cadence*** Design Entry CIS, the layout was created using PCB123, a free design program from the board fabricator ***Sunstone***. The revised board places components on both sides of copper clad FR-4. The board size is 4.5”x3” which was chosen to fit in a pre-existing circuit board box. The

layout itself can be shrunk considerably as the components used are surface mount. Extra area is used around the voltage regulators, as well as heat sinks, to reduce the ambient temperature of the board. Previous versions ran significantly above room temperature, which caused performance variation when the equilibrium shifted. By switching to only +/-5 volt regulators, the supply voltage was changed from +/-15 volts to +/-6 volts, which also reduced excess heat significantly. Components are placed on both sides of the board to allow easier power trace routing and to allow some signal trace crossover. Input and output connections are placed on opposite sides of the board, with a power connection at the center of another edge. The monitor port for the converted trigger signal is placed opposite of the power connector. Pictures of the PESU unit with components and of the closed box are given in Figure 22 and Figure 23.

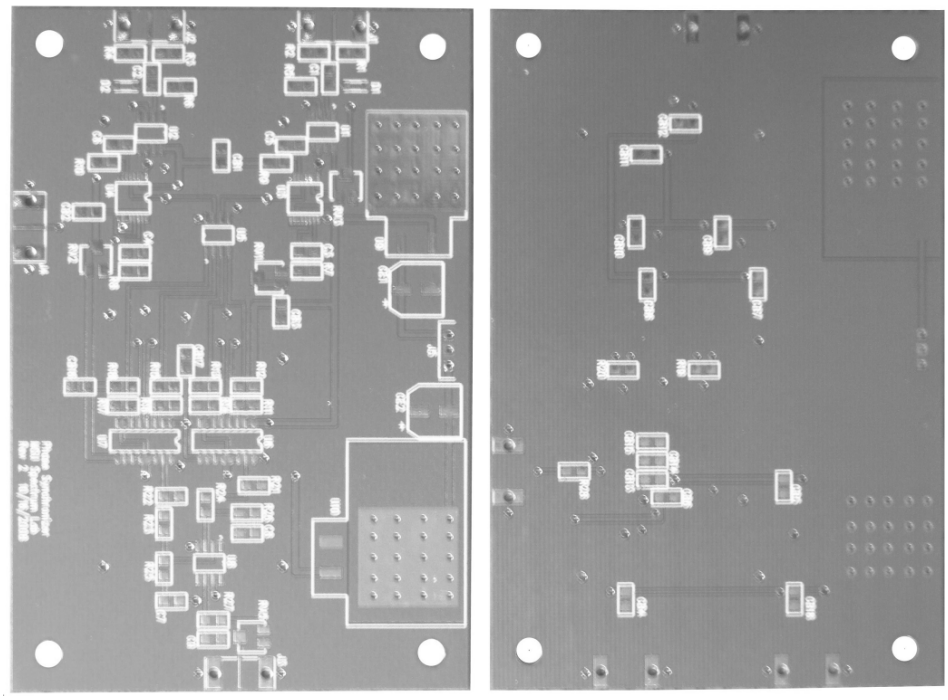


Figure 21: Final Revision of the Circuit Board (unloaded)

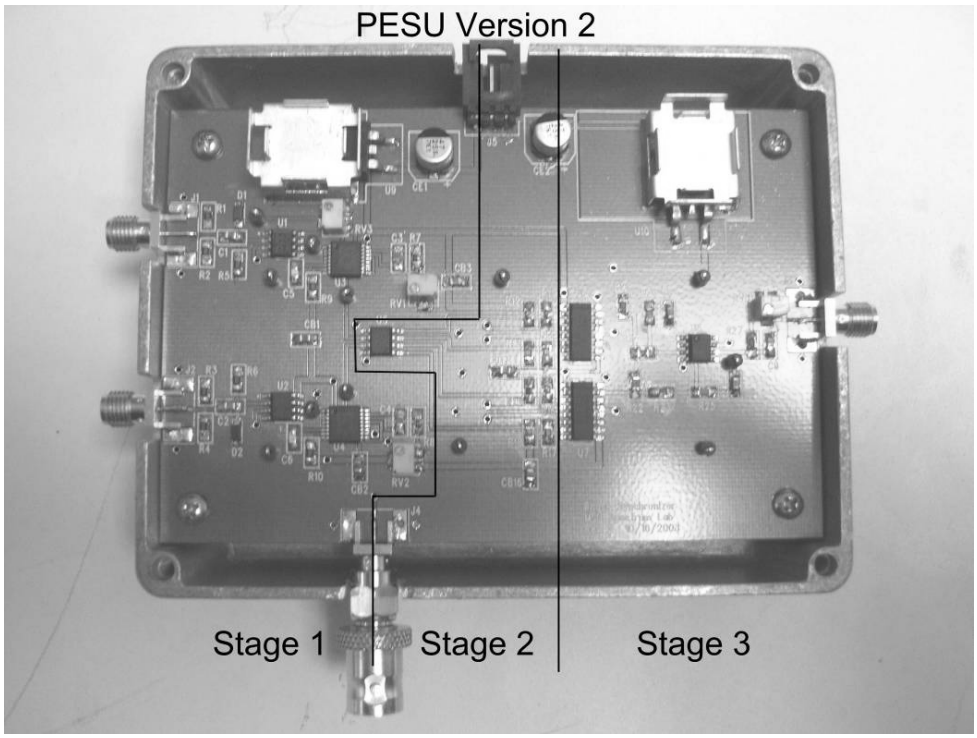


Figure 22: Final Version of PESU (loaded)

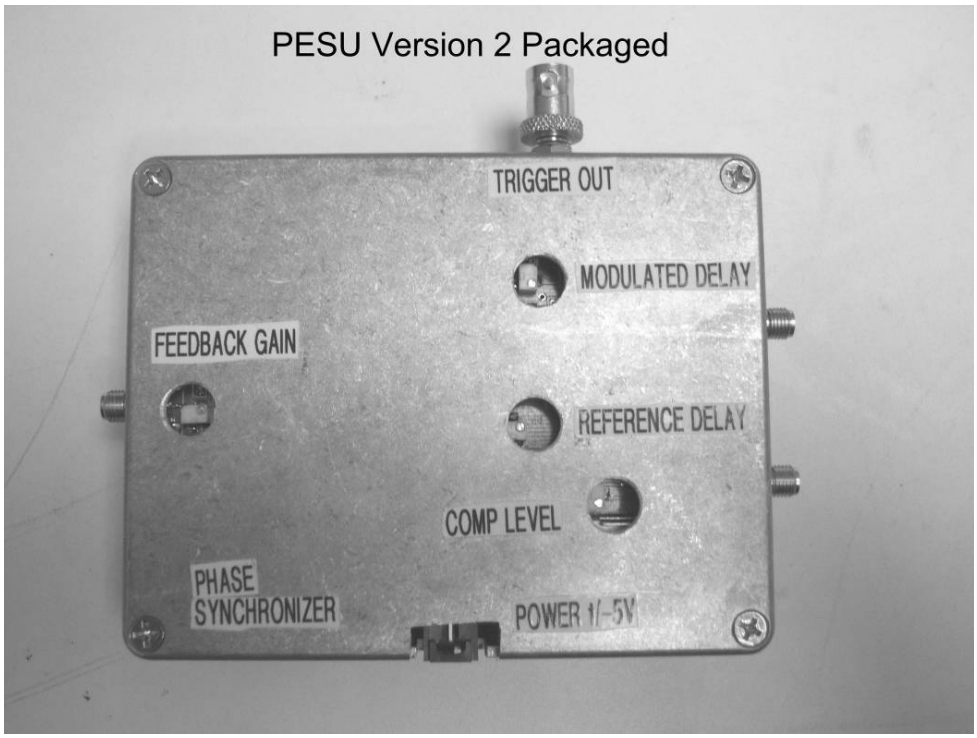


Figure 23: Labeled PESU Unit

SIMULATION OF DEVICE

Before the final revision of the board, a study was implemented to find circuit components for controlling the PESU performance. Adjustments to the bandwidth of the locking system allow for the system to be more versatile and help to minimize steady state error. To determine how adjustments to the loop filter affect system characteristics, the locking circuit was modeled in ***Cadence*** Design Entry CIS for the maximum data rates with 5GHz components. Initial loop filter parameters for the prototype were determined in ***MathCAD*** and those results are used to test the accuracy of the SPICE simulation model. Figure 24 gives the ideal form of the model employed in SPICE.

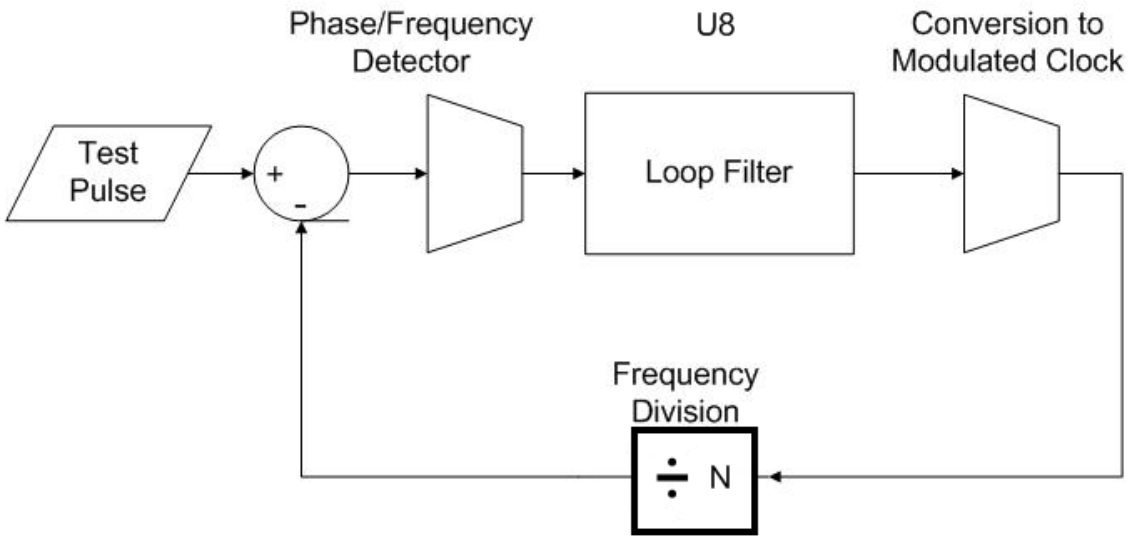


Figure 24: Ideal PESU Simulation Block Diagram

The model applies a step to the control loop error signal returned to the PFD. The step simulates an instantaneous change in the reference frequency while the returned error signal emulates the frequency difference between the initial reference trigger and

the modulated PPG trigger. The model shifts the magnitude of the triggers frequencies to zero to allow an initial operational feedback signal of 0 volt. The data stream frequency is scaled proportionately to maintain the overall model's frequency response. The loop filter adjusts the returned signal to cancel the disturbance. As this model is meant to model the loop filter, standard control function blocks are used as replacements for the surrounding system components, namely the phase lock loop (PLL) and the FM modulation of the slave PPG clocking source. Figure 25 is the actual SPICE circuit, with the loop filter enclosed in a separating box.

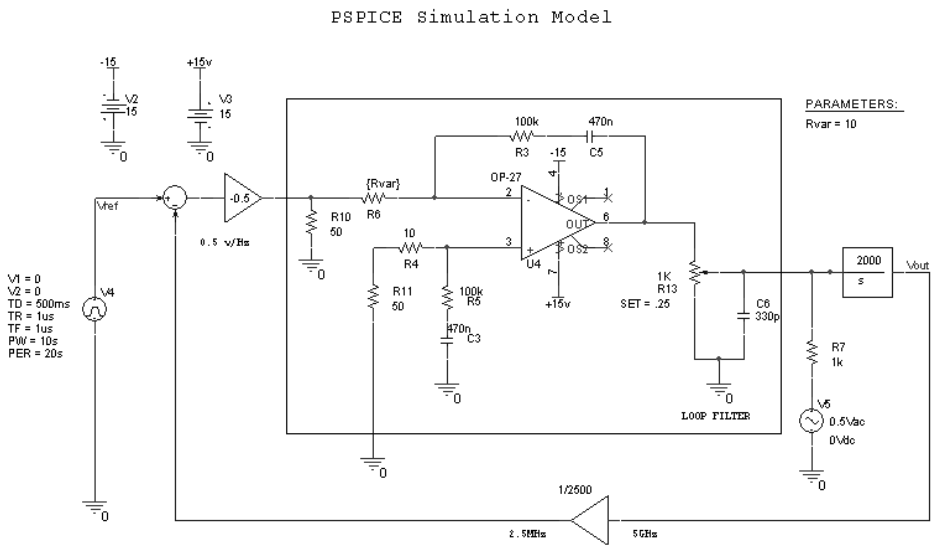


Figure 25: Actual SPICE Simulation Model of PESU in System

The transient response of the model is given in Figure 26. The disturbance to the system is a 2mV step at 500ms with rise and fall times of 1μs. This corresponds to an increase in the 5GHz carrier of 5kHz. The loop filter responds by altering the feedback to 5 volts to the 1000Hz/volt FM modulation. The divider, representing adjustment of the

data frequency to the PPG trigger frequency, reduces this to a 2mV signal to counter the disturbance. The response time of the loop filter to match the step impulse is on the order of 100ms. Anticipated disturbances between the two PPG clocks are on a scale of less than one Hz.

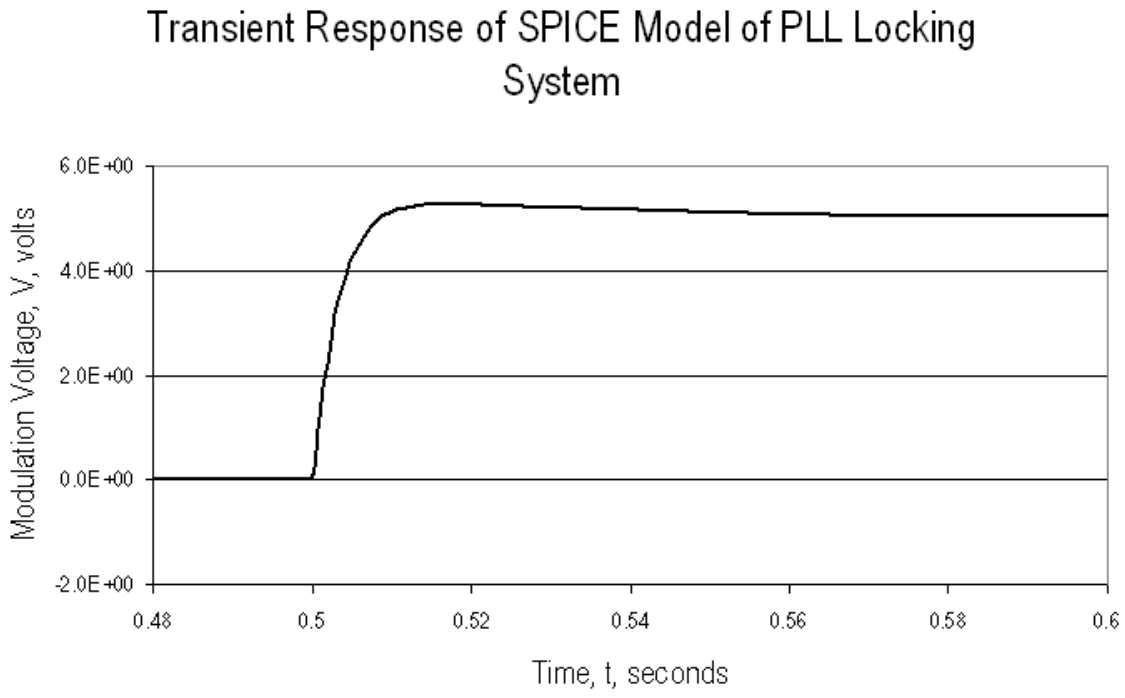


Figure 26: Modeled Transient Response of PESU in System

Figure 27 shows the results of the initial simulations in characterizing the device frequency response.

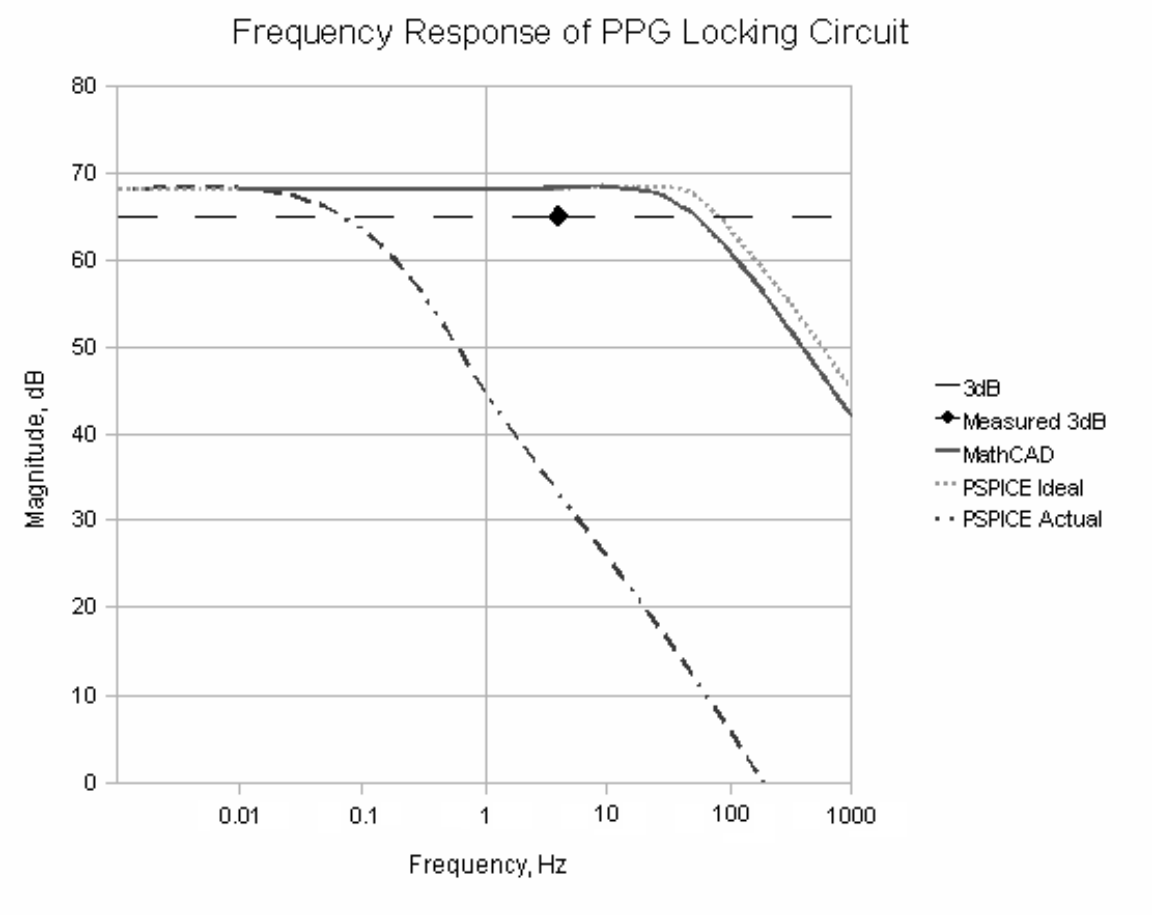


Figure 27: Closed Loop Frequency Response of PESU in System

The ***MathCAD*** model placed the 3dB point at approximately 55Hz. The PSPICE simulation using an ideal operational amplifier in the closed loop system model places the 3dB point at near 80Hz. These frequencies are close and provide evidence that the loop filter is being modeled adequately. When the model for the actual amplifier being used is substituted for the ideal amplifier, the 3dB frequency lowers by a factor of 1000 to 70mHz. This difference in frequencies is due to the input bias characteristics of the non-ideal amplifier. Changes to the loop filter model were made to attempt to compensate for the non-ideal nature of the amplifier but no changes allowed the model to

reach the ideal 3dB frequency. An addition of an operational amplifier pole may provide further correction and will be implemented if PESU redesign is undertaken. Measurements of the actual loop filter were taken to compare to the models and was found to be at approximately 4Hz. The amplifier operation does lower the 3dB frequency, but only by a factor of 10. An alternate amplifier model replaced the LF356 amplifier model in the simulation and the resulting 3dB frequency increased to 6Hz, which is much closer to the observed response. The results indicate that operational amplifier characteristics had a more significant effect on the loop filter response than the variations in resistor and capacitor values.

Direct measurement of the loop filter response was not possible in the system when operating normally. The adapted test system is shown in Figure 28. The response was determined by adding a sinusoidal voltage to the PESU's control signal as it modulated the slave PPG's clock through a fixed resistance. Outside of the system's bandwidth, the PESU cannot compensate for this modulation and the signal appears on the external PPG clock signal. By increasing the gain of the control loop, the 3dB loop bandwidth becomes higher in frequency. The model expects a linear relation between the gain and operating bandwidth; however, the real circuit deviates from linear response. Figure 27 displays the model's predicted bandwidth for different gains as well as the measured response.

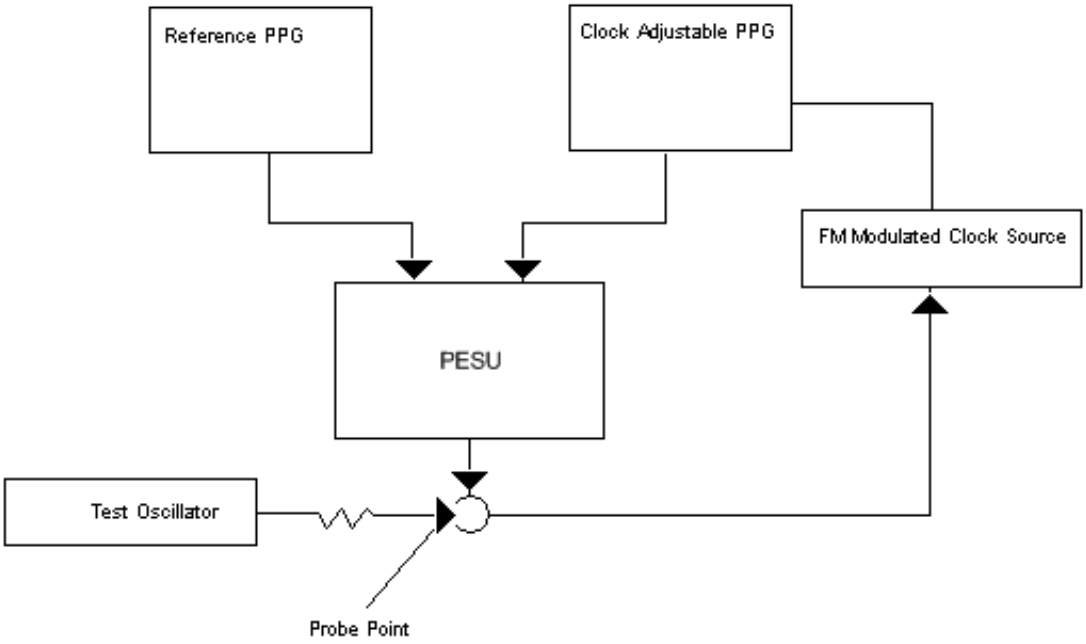


Figure 28: Setup for Testing the System Frequency Response

While the model is of the right order of magnitude of the actual bandwidths, considerable error is present. Figure 29 a shows plot of how the 3dB frequency varies as the open loop gain of the system is adjusted. This difference increases with gain and trying to increase the loop gain much further actually causes a decrease in bandwidth. This indicates that another system component acts to limit the 3dB bandwidth. Small changes in the supplied voltage to the PESU prototype also affect the system's 3dB response which indicates the PFD was another significant factor. The PFD IC is the only IC to operate on non-standard voltages. The bandwidth data was taken at the optimized voltage supply setting. The small offsets caused differences of two orders of magnitude. The operating voltage of the PFD has a strong effect on the absolute levels of the U and

D signals. This analysis is the primary reason for the change from the use of single ended U and D signals to converting the differential U and D signals before the integrator in the loop filter.

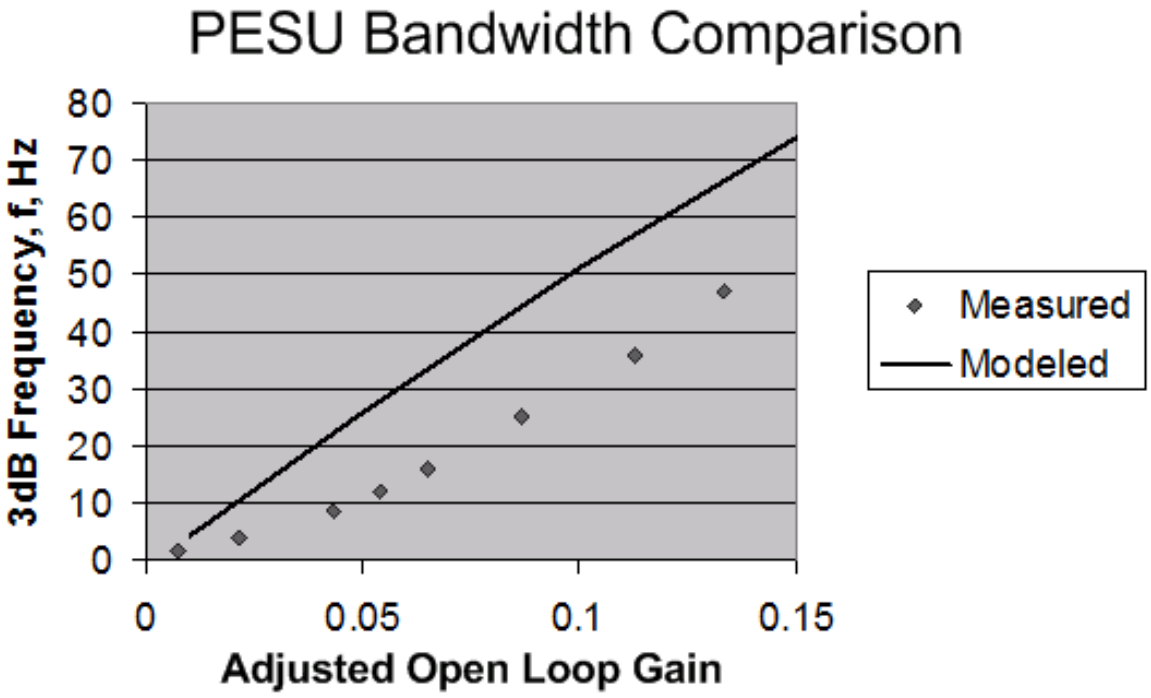


Figure 29: Comparison of Modeled and Observed System Closed Loop Bandwidth

DEVICE PERFORMANCE

System Setup

While the development of the PESU enables 20GBPS operation with older equipment, the size of the system is no longer compact. A photograph of the system is given in Figure 30. The PESU is connected to the system by coaxial cables from the pattern trigger ports on the PPGs and a cable linking the PESU output to the external input of the slave PPG clocking signal generator. The connectors of the cables are SMA in form and the cables are rated to 18GHz. While the pattern trigger repetition rate has a maximum of approximately 5MHz, the 18GHz aid in maintaining the sharp rising edge of the pulse. The PESU is powered by a DC supply set to +/-6 volts through three, twisted wires with banana plugs at the supply interface and a 3 pin Molex connection to the device. The other signal generator in the system supplies the clock to the MUX. The MUX interfaces with both PPGs and its clocking generator. The coaxial cable supplying the MUX clock is a testing cable rated to 36GHz. The PPG data lines are 18GHz matching coaxial lines of a length of 2 meters. The cabling of this setup is not ideal. Better performance can be achieved using cabling for the PPG data lines and the pattern triggers that is semi-rigid in nature. The standard, flexible cabling changes its characteristics when subjected to movement, such as vibration. Large movements cause enough change in the pulse edge of the PPG trigger signal for misalignment to occur. Rigid cabling addresses this issue, but it adds extra cost and does not allow for easy rearrangement of the system devices.

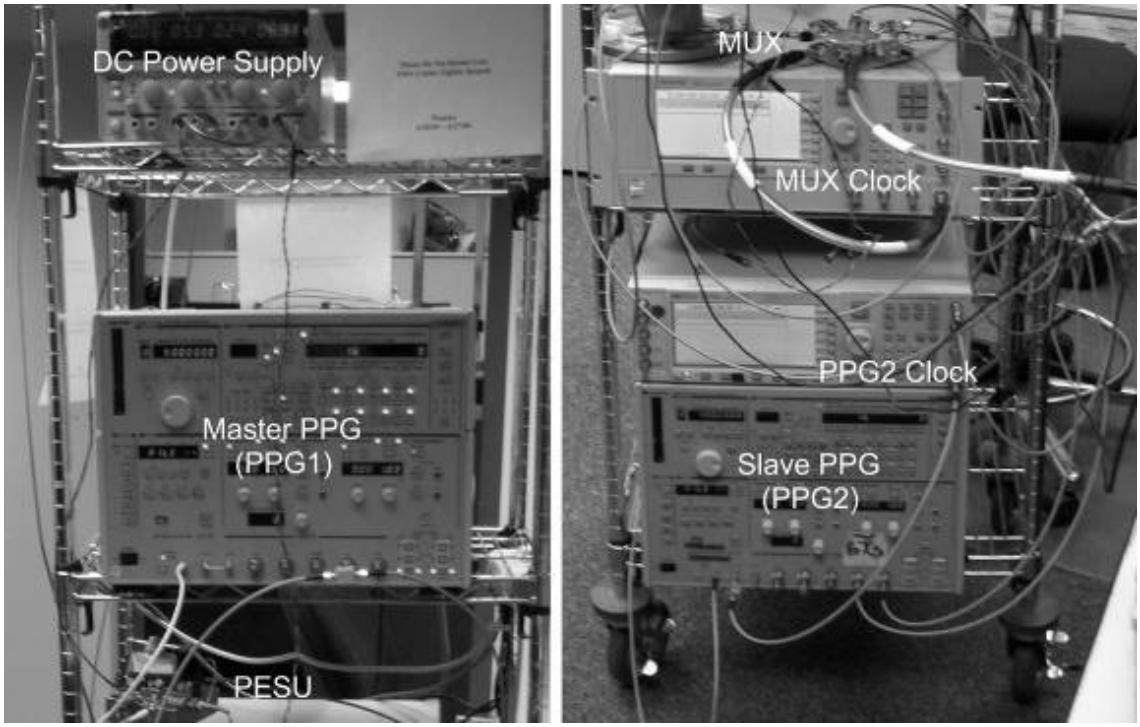


Figure 30: SSH-ADC Reference Signal System Setup

Device Operation

Figure 31 displays the initial misalignment of the pattern triggers at PPG startup. The traces are taken before the PFD at the outputs of U3B (channel 1) and U4B (channel 2) in the PESU and do not have the same phase offset at every startup. Once the feedback signal (channel 3) is FM modulated to the slave PPGs external clock, the traces align as in Figure 32.

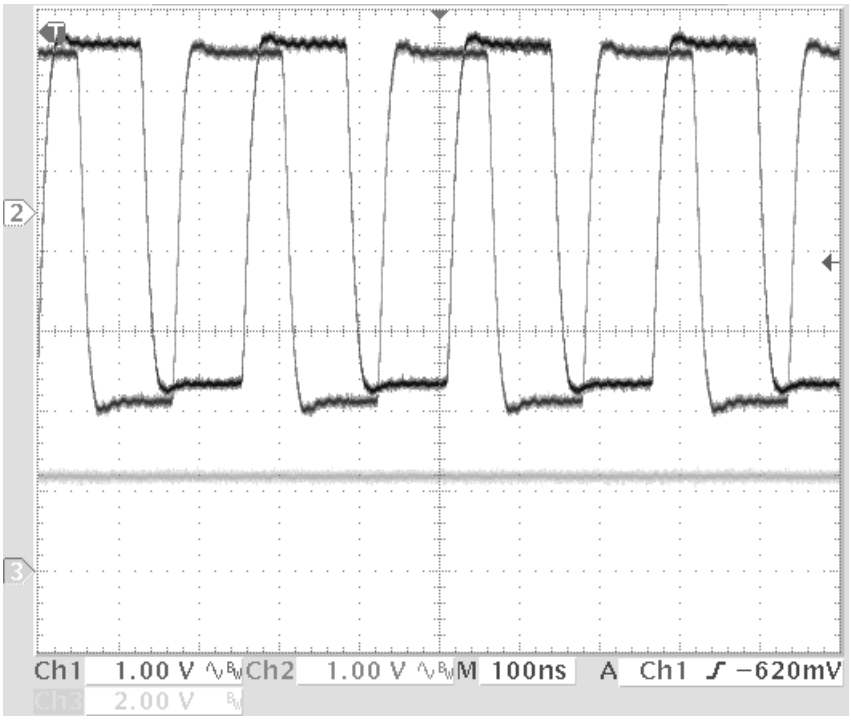


Figure 31: Pattern Trigger Misalignment at Equipment Start-up

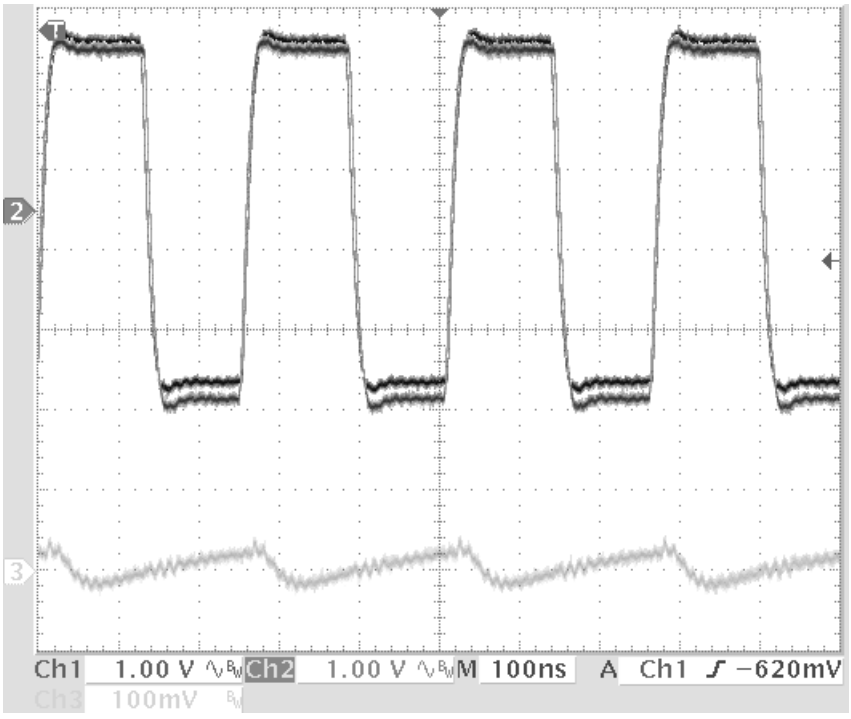


Figure 32: Pattern Trigger Alignment with PESU at 100ns per division

On the scale of the referenced traces, the alignment looks to be exact. Figure 33 provides a scope trace with a much smaller time scale. The slave PPG trace displays satisfactory alignment even on the 100ps time scale. Some oscillation initially occurred due to the steady state error of the control loop.

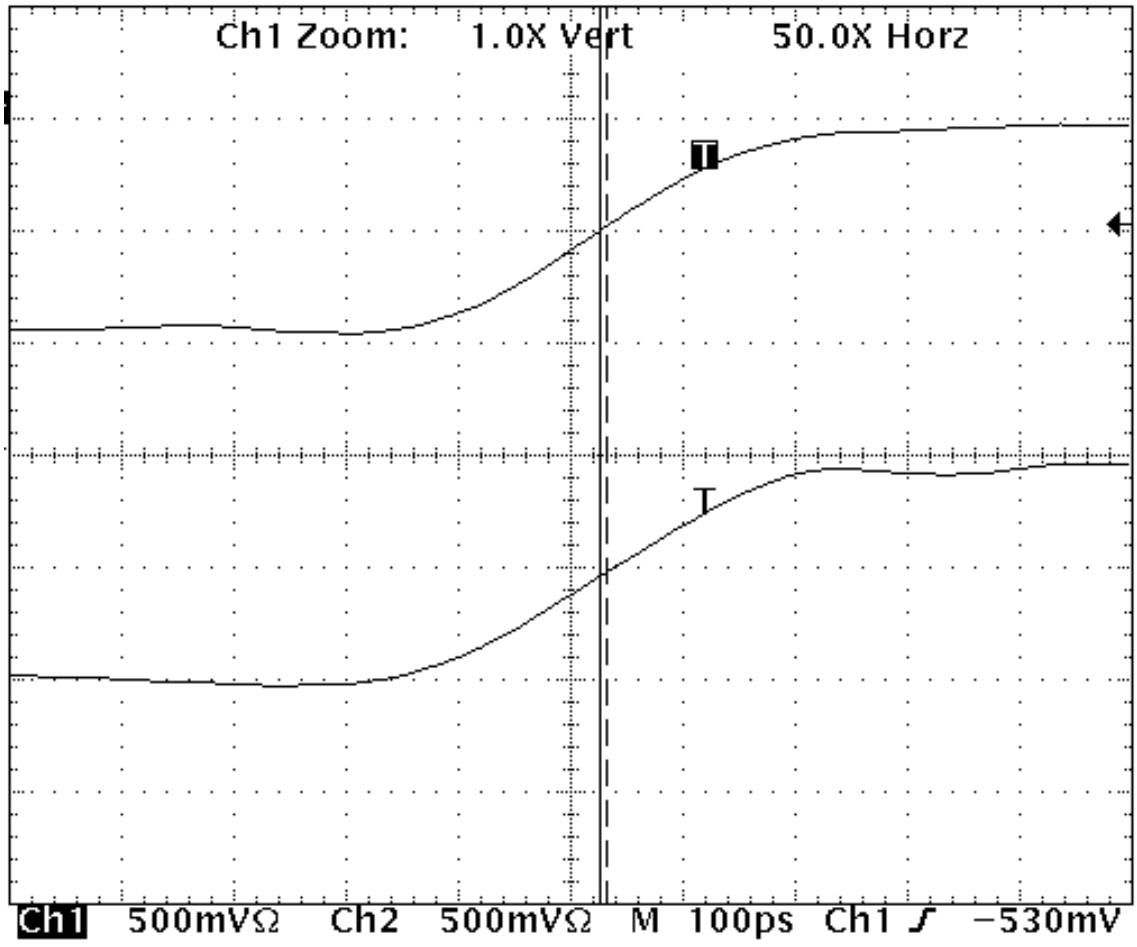


Figure 33: Pattern Trigger Alignment with PESU at 100ps per division

In addition to accurately aligning the triggers, the time taken to perform the alignment is of importance. The alignment time at device startup can be rather long, depending on the pattern length. For particularly long codes, several minutes may be

required for the trigger edges to precess to each other. The locking time can be decreased by increasing the control loop gain of the system by a factor of 100 temporarily, typically by increasing the FM deviation constant on the clock generator. Once the trigger pulses are in close proximity, the control loop gain is lowered to a suitable level for operation. The larger the control loop gain, the larger the steady state oscillation of the slave trigger pulse to the reference trigger pulse will be and can be enough to keep the PESU from achieving a consistent lock. Typically, the control gain is adjusted more for lower steady state error than faster response time. Disturbances to the trigger pulse edges tend to be small and large gains are not needed to correctly adjust the trigger alignment to maintain acceptable data pattern phase differences. Figure 34 contains a trace of the modulation signal as the triggers approach a lock position. When the trigger pulses are significantly apart, the modulation signal is maximized. The modulation signal responds exponentially with a slight overshoot when the pulses become close enough. Steady state error is always present between pulse edges. If error accumulation is large enough, the slave trigger edge will oscillate with respect to the reference trigger pulse. This effect becomes more evident at larger data pattern lengths, which cause lower pattern trigger repetition rates. When the time between trigger pulses lengthens, integration applies a larger error to the modulation signal before being corrected.

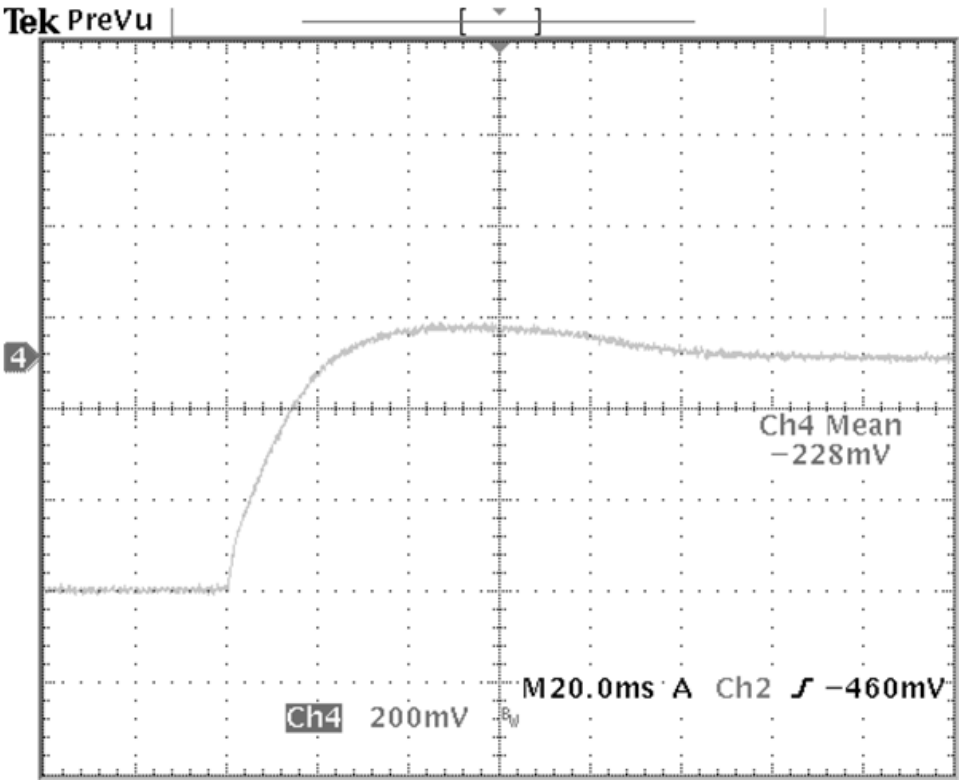


Figure 34: Modulation Signal from PESU during Trigger Phase Lock

While the trigger pulses are what the PESU directly acts on, the ultimate goal is the alignment of the data patterns, so the trigger signal delays must be adjusted to compensate for system delays. Figure 35 displays the synchronized data streams of the PPG1 and PPG2 data outputs, set to the same 16 bit pattern. A smaller time scale of the data patterns is shown in Figure 36 and displays a minimum misalignment for that pattern arrangement. The alignment is optimized by adjusting the delay between the trigger pulses, which counters differences in phase due to signal paths and equipment limitations. The correct amount of delay is not constant over time however, as temperature variations, vibrations, and device jitters continually vary the phase differences between the trigger pulse edges at the input to the PESU and the edge of the first bit in the data streams at the

oscilloscope. The PESU continually acts to align the trigger pulses to the set delay but does not automatically adjust that delay when small changes appear in the paths. This requires a manual adjustment of the PESU trigger pulse delay. This adjustment is not needed often once the system achieves an equilibrium temperature and cabling is not repositioned.

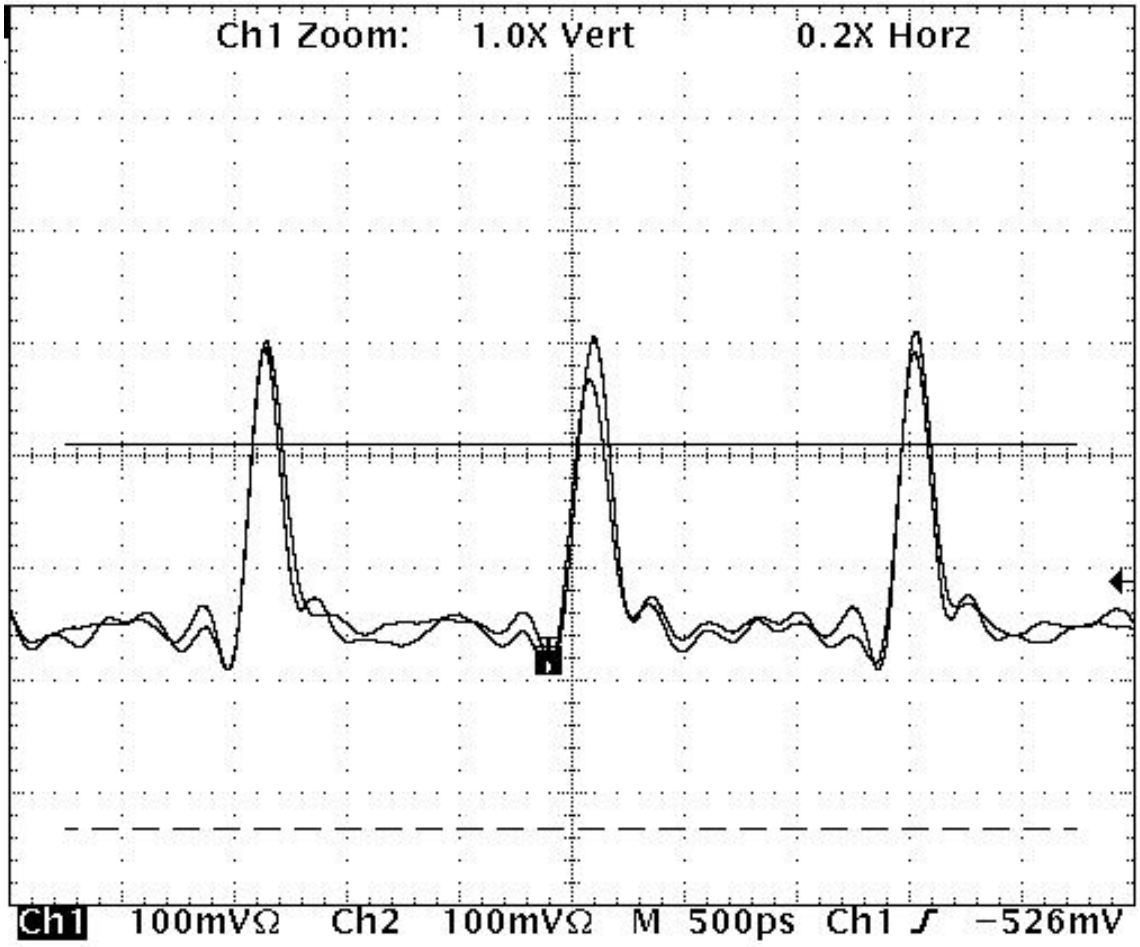


Figure 35: Full Pattern Data Alignment with PESU

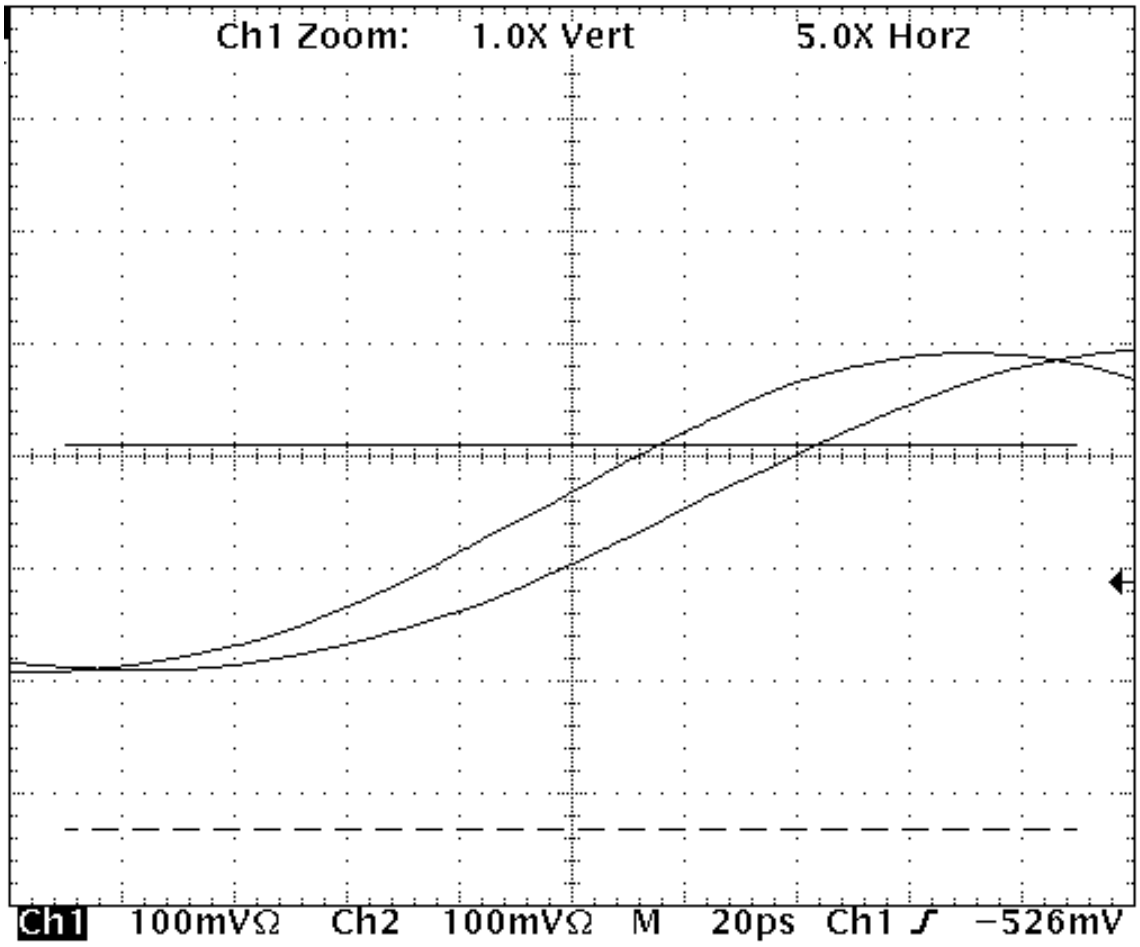


Figure 36: Minimum Achieved Data Edge Alignment

Figure 37 gives a random sampling of pattern misalignments over a period of an hour. While the data points show a very low frequency variation, the actual difference in pattern edges also varied on a far faster scale, alternating between negative and positive offsets in the course of seconds. Most important about the variation is the relation it has to the temporal position of the next bit in the data series. The difference between edges tends to be in the range of 50ps while the next bit in the pattern is 200ps. Keeping the edge difference much lower than the bit difference lowers the chance that the MUX will read an incorrect bit. Again, improvements to cabling reduce the amount of the absolute

phase variation. The time scale of the alignment required by the SSH-ADC experiment is on the order of 10ms, so slower drifts do not cause a significant impact.

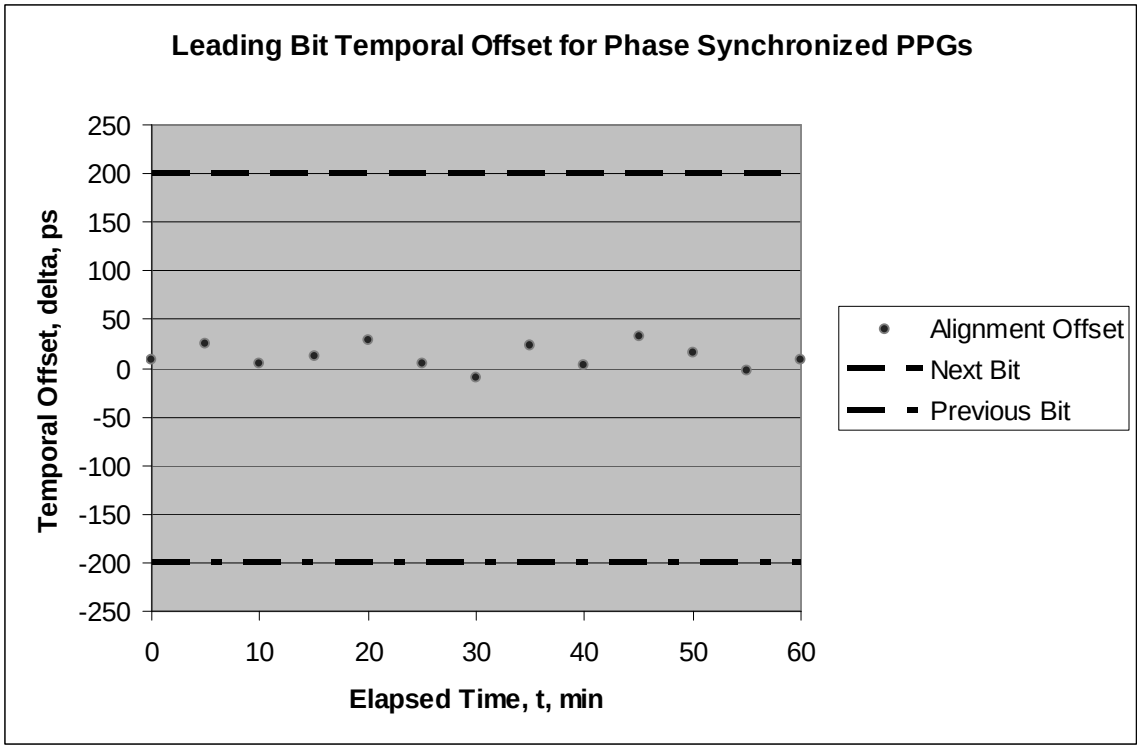


Figure 37: Bit Alignment Stability of PESU

System Operation

The true test of the PESU is in the performance of the system at the MUX output rather than the PPG data streams. The MUX operates by sampling and holding the signals applied to the inputs and then using a shift register to output the patterns at a rate of 20GBPS. This method of multiplexing has the advantage of not requiring extremely exact positioning of the 5GBPS data streams. This is evident when observing the output pattern as the trigger pulse delay is varied. There is a significant range of bit to bit delay

that allows stable operation. Optimally, the delay should be set to the middle of this range to guard against system disturbances.

The patterns used to test the MUX are given in Table 4. The channels are applied to the MUX such that the 20GBPS data stream has the following order: PPG1, $\overline{\text{PPG2}}$, $\overline{\text{PPG1}}$, PPG2.

Table 4: PPG Data Patterns for MUX Testing

PPG1 Data Pattern																
Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Value	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PPG2 Data Patterns																
Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pattern 1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Pattern 2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Eye diagrams of the MUX output are given in Figure 38 and Figure 39. While the pattern change to PPG2 could easily be accomplished by adjusting the trigger delay, for this test, the actual PPG data pattern was changed. This was to demonstrate that the lock of the PPG trigger pulses was not affected by changing individual bit values in a pattern. More significant changes, such as to bit rate or pattern length do require the PESU to reacquire the lock. The eye diagrams provide visual proof that the PPG data edge difference does not vary enough to cause slipped bits in the multiplexed output.

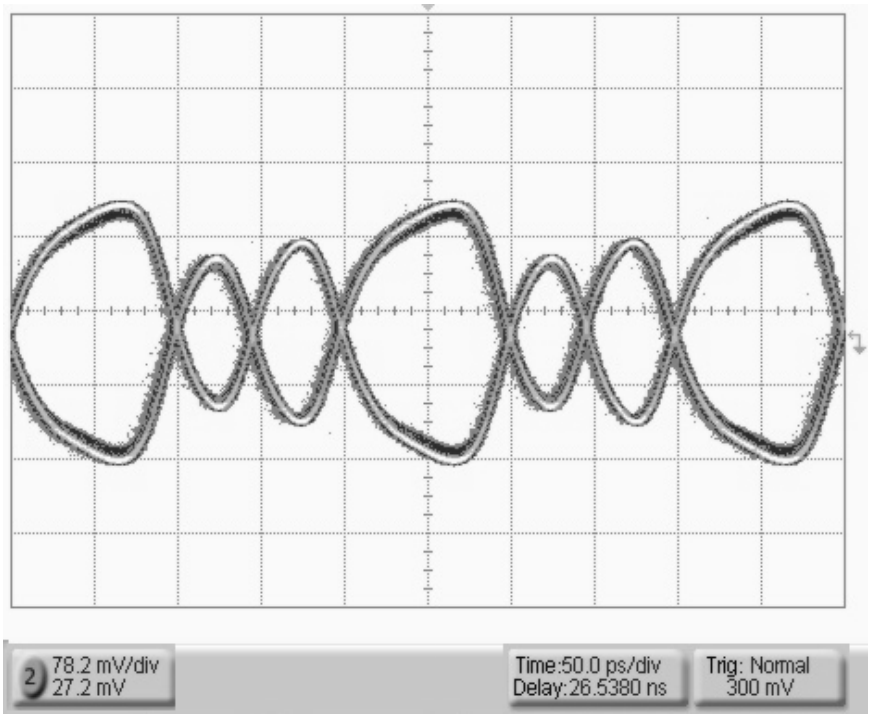


Figure 38: Eye Diagram of Multiplexed Pattern 1

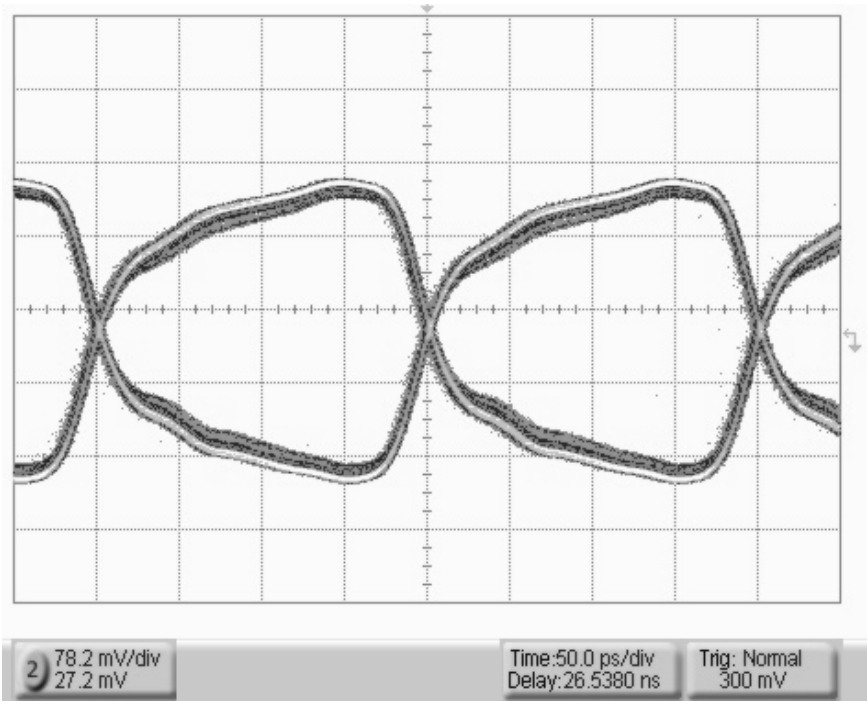


Figure 39: Eye Diagram of Multiplexed Pattern 2

From an eye diagram, the repeatability of the MUX signal can be quantified in terms of the jitter in the signal. By accumulating samples of a repeated data stream at regular intervals, the temporal position of that data stream with respect to the regular interval can be determined, which is known as the signal's jitter. Figure 40 displays a sampled pattern from the slave PPG data stream when triggered by the reference trigger signal from the PESU. The RMS jitter, width of the data pattern at mid level of the signal, varied from 3 to 7ps over 59 measurements. This timing error (or thickness in the observed eye diagrams) can be thought of as the temporal difference between PPG1 and PPG2. Figure 41 gives the jitter performance of the MUX output with respect to the MUX clock signal. The RMS jitter of the MUX output pattern is approximately 1ps, which is very close to the limits of the sampling oscilloscope.

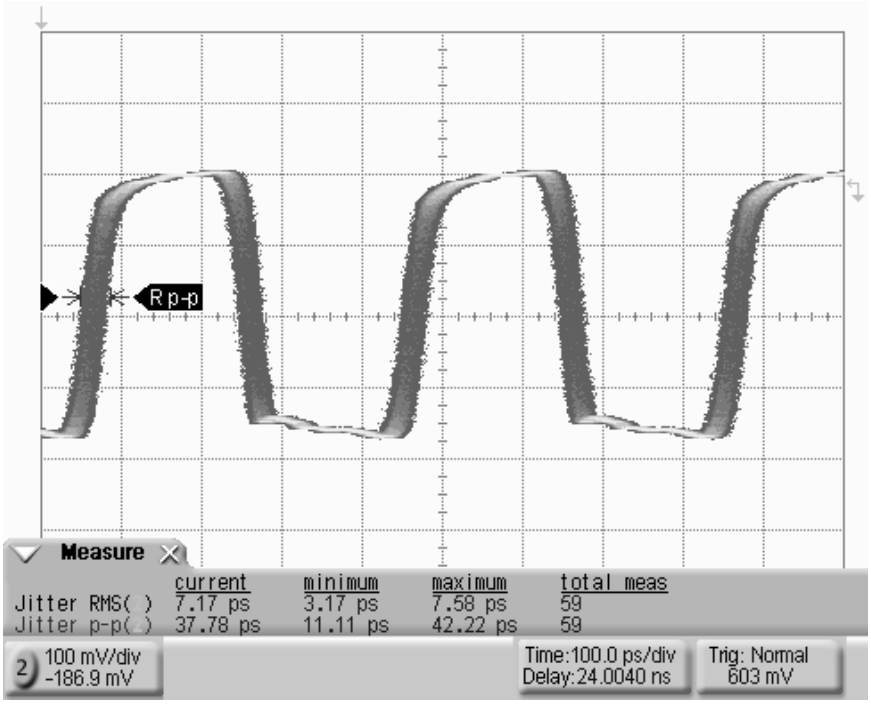


Figure 40: PPG Data Stream Jitter with Respect to the Reference Trigger Signal

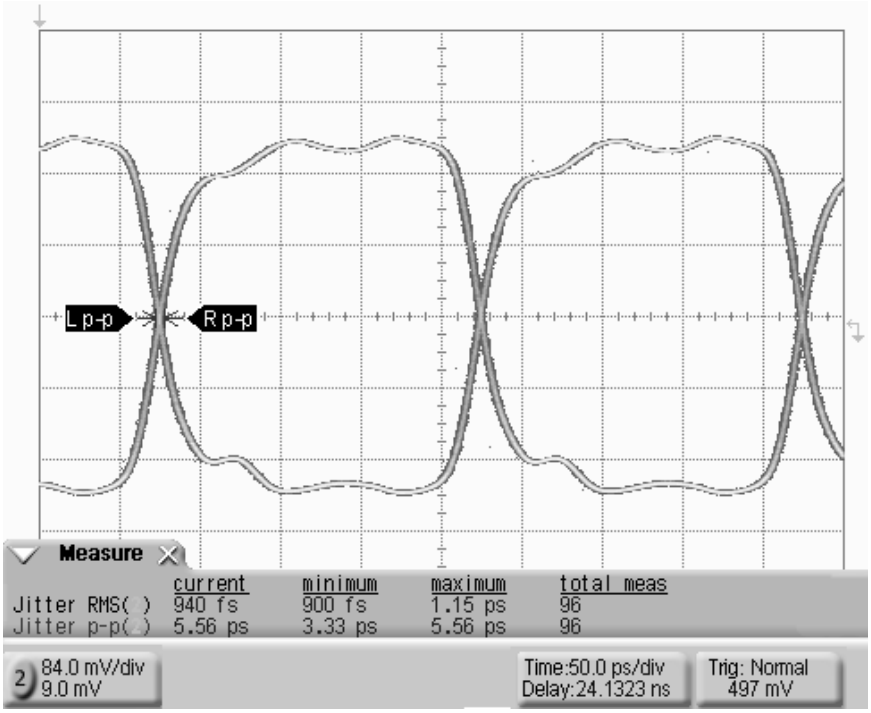


Figure 41: Multiplexed Data Stream with Respect to the Divided MUX Clock

From these two figures, it is clear that the jitter from the PESU alignment of the devices is not transferred through the MUX.

EXTENSION OF DEVICE FUNCTIONALITY

Alignment to Other Devices

Figure 42 displays an application made able by the changes in the latest revision to the PESU. This application involves synchronizing the slaved PPG to an alternate source operating at the same rate as the PPG pattern trigger.

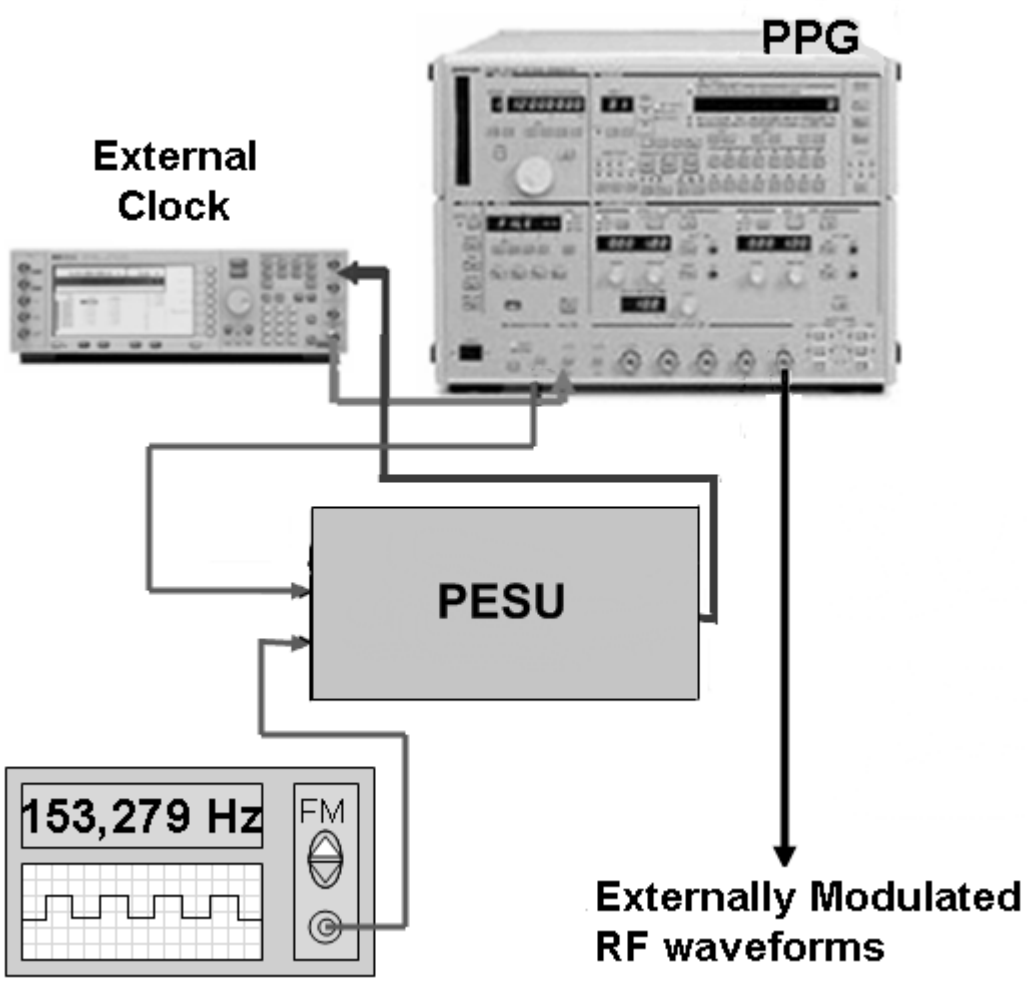


Figure 42: Proposed Set-up for External Pattern Data Frequency Modulation

The changes to the first stage of the circuit allow for this extension. The initial first stage was designed to act as a pulse stretcher for the particular form of the PPG pattern trigger. Other master trigger pulse sources would need to be adapted to be similar in levels to the PPG trigger to pass the transistor correctly. The change with the second revision uses a comparator to create a standard level trigger signal to be used for triggering the ICs requiring the wider triggering pulses. The setup used to test this functionality featured a signal generator set to the trigger pulse repetition rate. Various waveforms were used to verify that the PPG was able to align the data pattern start to a particular level of the master signal. The slave device is also not required to be a PPG, only that it can be clocked externally with a frequency modulated signal.

An interesting application of the setup in Figure 42 was using the PESU to synchronize the slave PPG to a master signal with a frequency modulation applied to it. With the pattern of PPG2 set to a simple square wave, the PESUs attempt to align to the modulated master signal reproducing the modulation on the data signal from the PPG. This shows that a set PPG pattern can be modulated based to an external source, which mimics the functionality of an expensive, commercially available add on module.

Arbitrary 20GBPS Code Production

The use of 5GBPS data patterns to form complimentary codes at 20GBPS for a seed pattern utilizing the PPG1 and $\overline{\text{PPG1}}$ channels is suitable for the reference signal generation. However, being able to create arbitrary 20GBPS complimentary codes with

the equipment available is highly desirable. Since each PPG can produce data streams up to 12GBPS, enough arbitrary bits are available to produce a 24GBPS signal, if they can be multiplexed. The ***Inphi*** MUX is designed to only accept four 5GBPS data streams. However, a simple 2 bit serial to parallel converter could transform the two 10GBPS data streams available into the needed four 5GBPS data streams. Figure 43 gives a way the arbitrary signal can be accomplished utilizing the PPG1 and $\overline{\text{PPG1}}$ in a single ended fashion.

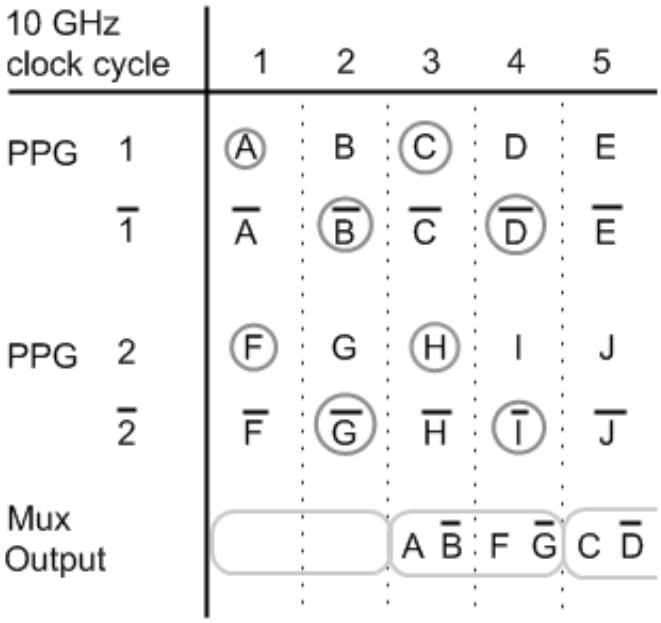


Figure 43: Timing Diagram for Arbitrary 20GBPS Signal Production

The circuit to divide the two 10GBPS data streams is rather simple and a generic diagram is given in Figure 44. The DFF will need to operate at 5GHz and the clock can be supplied by the MUX as it has an output of its clock divided by four. Additional ICs will be needed to provide enough branches of the clock signal to drive eight DFFs. The

components for such a converter are chosen and the circuit board is currently being designed.

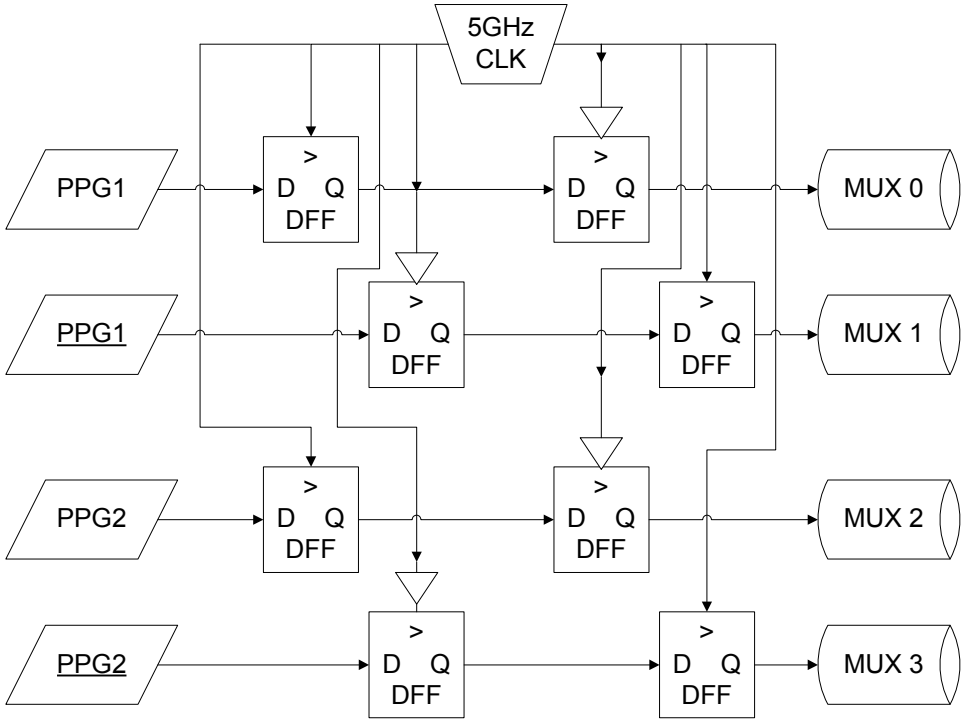


Figure 44: Serial to Parallel Conversion Circuit

CONCLUSIONS

The primary design goal for the device featured in this thesis is to provide an inexpensive way to create 40GBPS binary data streams that can take the form of complementary sequences. Using a relatively inexpensive multiplexer, a proof of concept system was built and the system delivered the reference signal needed. The system operates using a less expensive, 20GBPS multiplexer available in-house at Montana State University Spectrum Lab and can be upgraded to function at 40GBPS by replacing the MUX and its clock with the equivalent 40GBPS ***Inphi*** MUX and a 40GHz clocking source. The other in-house pieces of the proof of concept system consist of two 12GBPS PPGs operating at 5GBPS, a signal generator capable of producing a 5GHz, frequency modulated signal, and a 20GHz clock source. Due to PPG limitations, the PESU is needed to provide the ability to align the PPG data streams for correct multiplexing.

The PESU and external PPG frequency modulated clock source operate in the system as a phase locked loop. The unit takes as input two pulse streams from the PPGs, each marking the beginning of its PPG's output data stream. The unit converts the input pulses into a reference signal from the master PPG and a modulated signal from the slave PPG, both of which are optimized for use by the PESU's onboard PFD. The PFD receives these signals and produces two output signals, U and D, such that the difference between U and D is directly proportional to the phase difference of the reference and modulated signals. The final action of the PESU is to integrate the difference of U and D and output that difference as a control signal. The control signal is then fed to the slave

PPG's RF signal generator to be frequency modulated onto the clock signal it provides the slave PPG.

The overall function of PESU is to cause slight frequency differences between the master and slave PPGs which cause the slave data stream to precess with respect to the master data stream. Once the streams are aligned, the control signal from the PESU approaches zero volts and both PPGs operate at identical clock frequencies. Once locked, the control loop of the system acts to correct disturbances occurring at frequencies of 10 Hz or less. Compared to the operating frequencies of the other components of the system, this frequency is extremely small and can be this small due to the stability of the PPG clocks. The circuitry operating at such low frequencies is far easier to implement and components are less expensive than existing solutions.

With the PESU, the proof of concept system produced 20GBPS complementary data streams in a triggerable and reliable fashion. Added jitter to the slave PPG data stream by the PESU was not reflected in the MUX output, only having the effect of bit order instability if the slave PPG jitter became a significant portion of the data stream pulse width.

The final version of the PESU offers several additional features. The improved trigger pulse manipulation stage provides the ability to align the PPG to other equipment with different event signal forms. Use of RMMs instead of DFFs improves the range and accuracy of the offset delay that can be applied to PPG data stream positioning, enabling the slave data stream to lead or lag the reference by up to 50ns. Changes to chip operating voltages allows for fewer voltage regulators and cooler board temperatures,

improving alignment stability. Adding differential to single ended amplifiers to change the differential U and D signals from the PFD lowers the error present in integration due to mismatches in the U and D absolute high and low voltages. Finally, the addition of a reference trigger signal output prior to the PFD enables several PESU devices to easily align more than two devices.

While operating satisfactorily for the proof of concept from the SSH-ADC project, there are improvements that can be made to the system. The size of the PPGs and signal generators requires cabling being longer than ideal. The current flexible cables should be replaced with semi-rigid cables to improve phase stability of the routed data and pulse streams. Use of semi-rigid cables limits will force components to maintain particular positions and orientations to prevent repeated cable shaping. There are two improvements that can be made to the PESU unit itself. First, multiple PESU circuits can be combined on one board, allowing multiple device alignment without added errors of cabling several of the current boxes together. Second, the variable resistors providing the reference and modulated signal delay adjustment could be replaced with larger footprint versions to provide easier adjustment. Both of these improvements would require a new board layout.

REFERENCES CITED

[1] Demonstrations of analog-to-digital conversion using a frequency domain stretched processor, ***Montana State University Spectrum Lab***, (2008), pages therein

[2] SHF 56 Gbps BERT Product Overview, ***SHF Communication Technologies AG***, (2009), 2

[3] 5080MX 50GBPS 4:1 Multiplexer, ***Inphi Corporation***, (2009), 1

[4] High-Performance Phase-Locked Loop TLC2933, ***Texas Instruments***, (1996), 1

[5] RF PLL Frequency Synthesizers ADF4116/ADF4117/ADF4118 rev D, ***Analog Devices***, (2007), 1

[6] Radar Handbook Second Edition, Skolnik M, (1990), 10.21

[7] ECL/PECL Phase-Frequency Detectors 19-2234, ***Maxim IC***, (2002), 8

[8] D3186 Pulse Pattern Generator Operation Manual, ***Advantest Corporation***, (1994), 12-1

[9] D3186 Pulse Pattern Generator Operation Manual, ***Advantest Corporation***, (1994), 8-8

[10] D3186 Pulse Pattern Generator Operation Manual, ***Advantest Corporation***, (1994), 8-7

[11] ECL/PECL Phase-Frequency Detectors 19-2234, ***Maxim IC***, (2002), 1

[12] ECL/PECL Phase-Frequency Detectors 19-2234, ***Maxim IC***, (2002), 8

[13] Agilent ESG Family of RF Signal Generators, ***Agilent Technologies***, (2003), 4

[14] 2080MX_DS_Ver1.0, ***Inphi Corporation***, (2006), 1

[15] 2080MX_DS_Ver1.0, ***Inphi Corporation***, (2006), 4

[16] Agilent 83751A/B and 83752A/B Synthesized Sweepers, ***Agilent Technologies***, (2002), 1

[17] Phase-Locked Loop Design Fundamentals AN535, ***Motorola***, (1994), 2

[18] 74LV123 Dual Retriggerable Monostable Multivibrator with Reset, ***Phillips Semiconductor***, (1998), 10

[19] ECL/PECL Phase-Frequency Detectors 19-2234, ***Maxim IC***, (2002), 7

[20] Phase-Locked Loop Design Fundamentals AN535, ***Motorola***, (1994), 7

[21] Phase-Locked Loop Design Fundamentals AN535, ***Motorola***, (1994), 4

[22] Phase-Locked Loop Design Fundamentals AN535, ***Motorola***, (1994), 6

APPENDICES

APPENDIX A

REVISION 2 PESU CIRCUIT SCHEMATIC

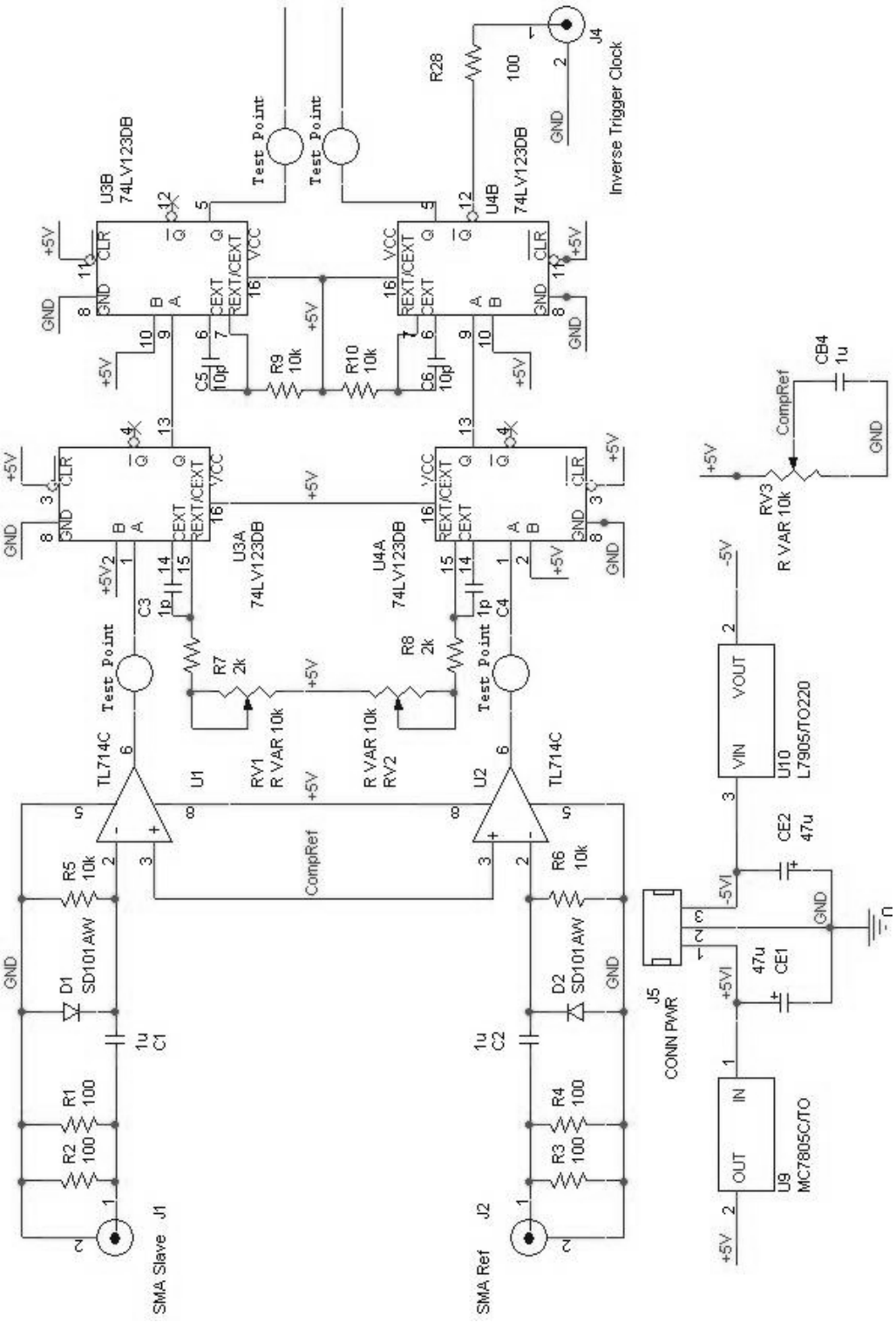


Figure 45: PESU Circuit Schematic Part 1 (left side)

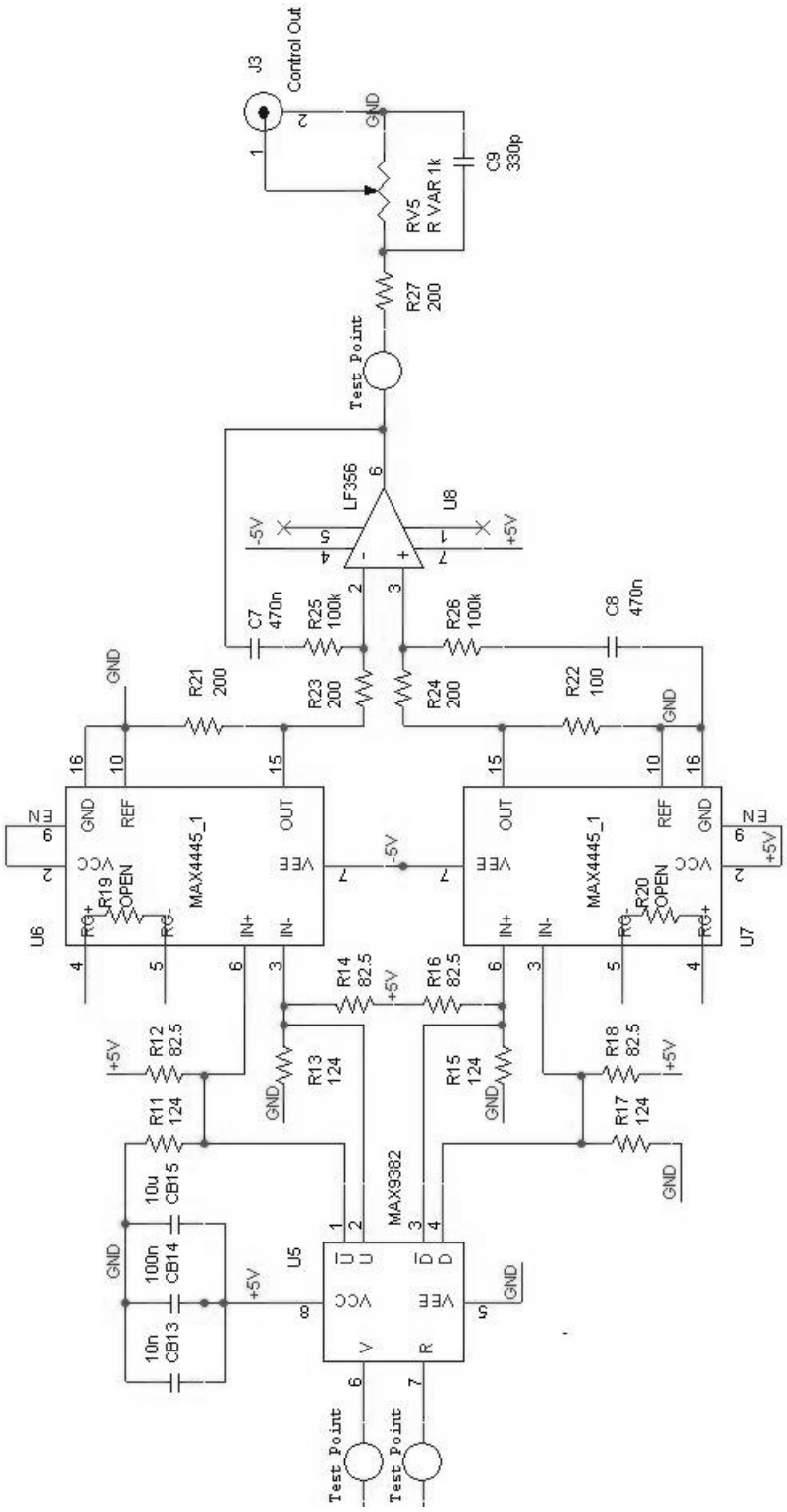


Figure 46: PESU Circuit Schematic Part 2 (right side)

APPENDIX B

REVISION 2 PESU BOARD LAYOUT

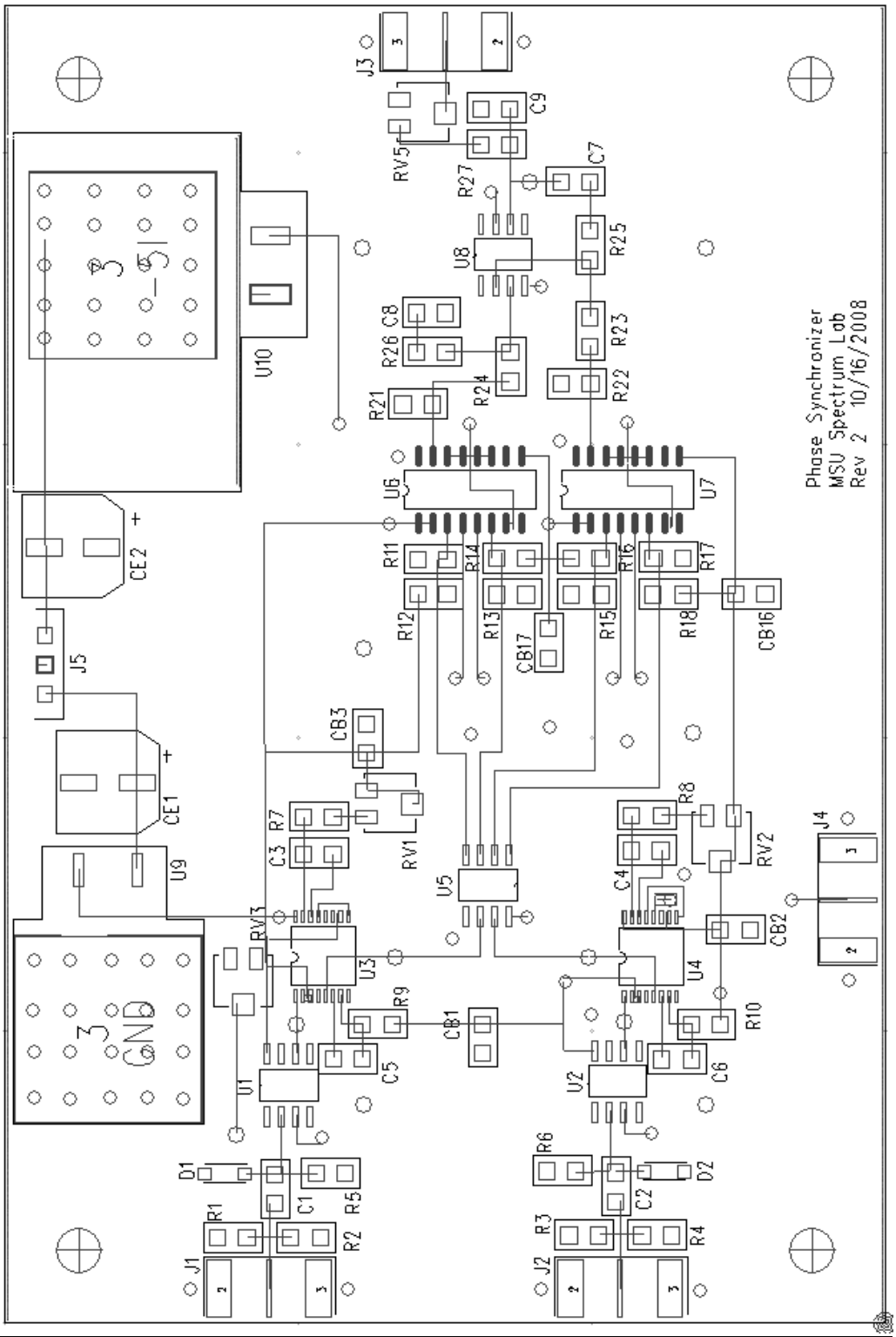


Figure 47: PESU PCB Top from PCB123

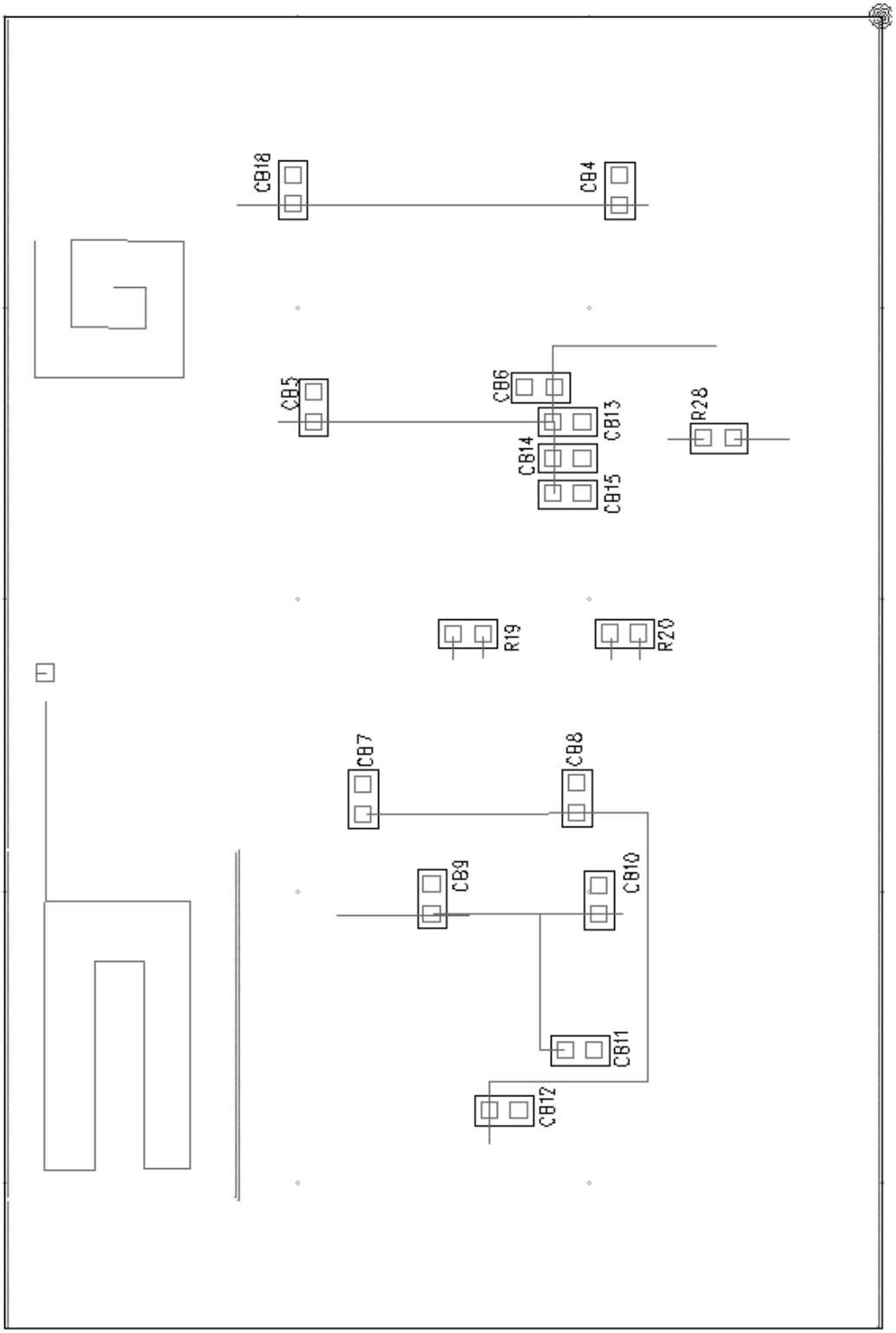


Figure 48: PESU PCB Bottom from PCB123

Table 5: PESU Part List

Part	Digikey Part#	Qty	Footprint	Board ID
SM Resistor 82.5	RHM82.5CCT-ND	4	805	R12,14,16,18
SM Resistor 100	541-100CCT-ND	10	805	R1-4,13-16,28,29
SM Resistor 120	541-120CCT-ND	1	805	R27
SM Resistor 124	RHM124CCT-ND	4	805	R11,13,15,17
SM Resistor 200	RHM200CRCT-ND	4	805	R21-24
SM Resistor 2k	541-2.00kCCT-ND	2	805	R7,8
SM Resistor 10k	541-10.0kCCT-ND	4	805	R5,6,9,10
SM Resistor 100k	541-100kCCT-ND	2	805	R25,26
OPEN		2	805	R19,20
SM Pot 1k	490-2660-1-nd	3	PVG5A	RV3-5
SM Pot 10k	490-2661-1-nd	2	PVG5A	RV1,2
SM Capacitor 1p	PCC010CNCT-ND	2	805	C3,4
SM Capacitor 10p	399-1108-1-ND	2	805	C5,6
SM Capacitor 330p	PCC1982CT-ND	1	805	C9
SM Capacitor 10n	PCC103BNCT-ND	1	805	CB13
SM Capacitor 100n	PCC1828CT-ND	1	805	CB14
SM Capacitor 470n	PCC2456CT-ND	2	805	C7,8
SM Capacitor 1u	PCC2319CT-ND	14	805	C1,2,CB1-12,16-18
SM Capacitor 10u	PCC2400CT-ND	1	805	CB15
Schottky Diode SD101AW	SD101AWTPMSCT-ND	2	SOD123	D1,2
Diff Comp TL714CD	296-6631-5-ND	2	SOIC8	U1,2
MultiVib 74LV123DB	74LV123DB (Arrow NAC)	2	SSOP16	U3,4
Phase Detector MAX9382	MAX9382ESA+ (***Maxim***IC)	1	SOIC8	U5
Diff-Single End MAX4445	MAX4445 (***Maxim***IC)	2	SOIC16	U7,8
Op Amp LF356	LF356M-ND	1	SOIC8	U8
+5V Reg MC7805	MC7805CD2TGOS-ND	1	D2PAK	U9
-5V Reg L7905	497-1214-1-ND	1	DPAK	U10
SMA PCB Board Launch	J629-ND	4	SMA End	J1-4
Power Connector		1	Molex-3	J5

APPENDIX C

MATLAB SCRIPTS FOR DETERMINING COMPLEMENTARY CODE SEED

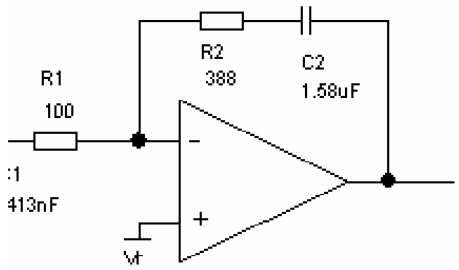
```
function [CompA,CompB] = compseq(n);

%CompA = [1 1 1 0 0 1 1 1 0 1 0 0 0 0 0 1 0 1 1 0 0 1 0 0 0 0];      %Complementary
Sequence A
%CompB = [0 0 0 1 1 0 0 0 1 0 1 1 0 1 0 1 0 1 1 0 0 1 0 0 0 0];     %Complementary
Sequence B

% Lets try to generate some longer sequences.

%close all

[CompA,CompB] = CompGen(n);

size(CompA)

figure
plot(CompA,'green')
hold
plot(CompB)

N = 100000;
E1=zeros(1,N);
E2=zeros(1,N);
E1(1:2^(n)) = CompA;
E2(1:2^(n)) = CompB;

%NY1 = 2*CompA-1;     %Conversion to -1,1
PP1= xcorr(E1) ;    %Autocorrelation of Seq A
%NY2 = 2*CompB-1 ;    %Conversion to -1,1
PP2= xcorr(E2);     %Autocorrelation of Seq B
Sum = PP1 + PP2 ;    %Sum of the correlation functions
figure
plot(PP1.^1./max(PP1.^1),'g')
hold on
plot(PP2.^1./max(PP2.^1),'r')

figure
plot(Sum.^2/max(Sum.^2)) % Field  must square for power.
```

```
function [Sf,Sfc] = CompGen(n)

S0 = [1];%[1 1 1 -1 -1 1 1 1 -1 1 -1 -1 -1 -1 -1 1 -1 1 1 -1 -1 1 -1 -1 -1 -1];
%[1];  %Seed

S1 = [S0,S0];
S1c = [S0,-S0];

Sf = [S1,S1c];
Sfc = [S1,-S1c];

for i=1:(n-2)
   Sfo = Sf;
   Sf = [Sf,Sfc];
   Sfc = [Sfo,-Sfc];
end
```

APPENDIX D

MATHCAD SCRIPT FOR ADJUSTING PLL LOOP FILTER

Estimation of a model for the phillips pll ic.
Author: AVO/RS 05/28/04
filename:[pll_ppglock.xmcd Last revision:12/18/07



**********set up log frequency sweep
****

$N := 1000 \qquad i := 0..N \qquad f_{lo} := 10^{-1} \qquad f_{hi} := 10^{3}$

$\Delta f := \frac{\log(f_{hi}) - \log(f_{lo})}{N} \qquad f_i := 10^{i \cdot \Delta f} \cdot f_{lo} \cdot Hz \qquad s_i := j \cdot 2 \cdot \pi \cdot f_i$

**********frequency constants **********

$f_0 := 5000 \cdot MHz \qquad f_r := 5MHz \qquad K_{vco} := 1000 \cdot \frac{Hz}{V} \qquad N := \frac{5000}{2}$

$K := 1$

$R1 := 200\Omega \qquad R2 := 100K\Omega \qquad C1 := 470nF \qquad K_p := \frac{.56}{4\pi} \cdot \frac{V}{rad} \qquad pot := .15$

$H(s) := \frac{1 + s \cdot R2 \cdot C1}{s \cdot R1 \cdot C1} \cdot pot$

$CL(s) := \frac{K_p \cdot \frac{K_{vco}}{s} \cdot H(s) \cdot K}{1 + \frac{K_p}{N} \cdot \frac{K_{vco}}{s} \cdot H(s) \cdot K} \qquad CL_i := CL(s_i)$

$OL(s) := \frac{K_p}{N} \cdot \frac{K_{vco}}{s} \cdot K \cdot H(s) \qquad OL_i := OL(s_i)$